

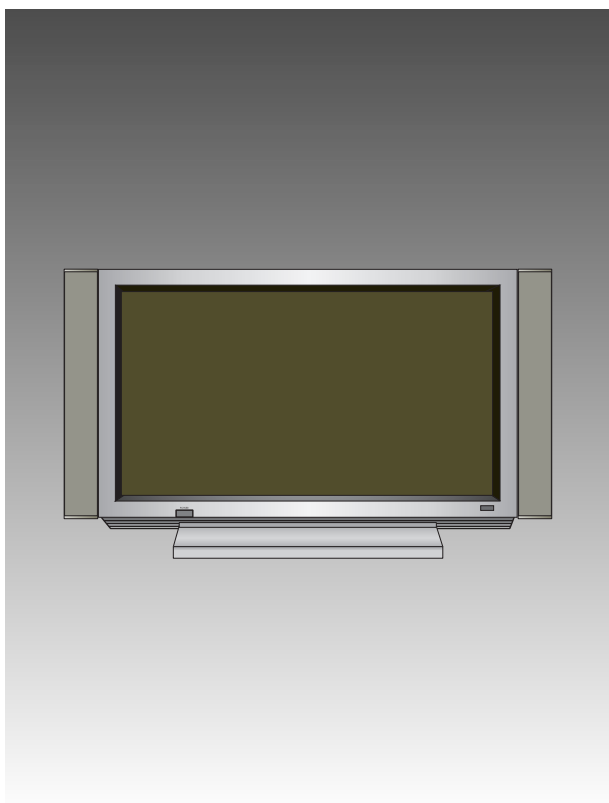
SAMSUNG

PLASMA DISPLAY TV

Chassis : D53A
Model: PPM42S2X/XAA

SERVICE *Manual*

PLASMA DISPLAY TV



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ELECTRONICS

1. Precautions

Follow these safety, servicing and ESD precautions to prevent damage and protect against potential hazards such as electrical shock and X-rays.

1-1 Safety Precautions

1. Be sure that all of the built-in protective devices are replaced. Restore any missing protective shields.
2. When reinstalling the chassis and its assemblies, be sure to restore all protective devices, including: nonmetallic control knobs and compartment covers.
3. Make sure that there are no cabinet openings through which people—particularly children—might insert fingers and contact dangerous voltages. Such openings include the spacing between front cabinet and back cabinet, excessively wide cabinet ventilation slots, and improperly fitted back covers.
4. Leakage Current Hot Check (Figure 1-1):
Warning: Do not use an isolation transformer during this test. Use a leakage-current tester or a metering system that complies with American National Standards Institute (ANSI C101.1, Leakage Current for Appliances), and Underwriters Laboratories (UL Publication UL1950.5.2).
5. With the unit completely reassembled, plug the AC line cord directly into the power outlet. With the unit's AC switch first in the ON position and then OFF, measure the current between a known earth ground (metal water pipe, conduit, etc.) and all exposed metal parts, including: antennas, handle brackets, metal cabinets, screwheads and control shafts. The current measured should not exceed 3.5 milliamp. Reverse the power-plug prongs in the AC outlet and repeat the test.

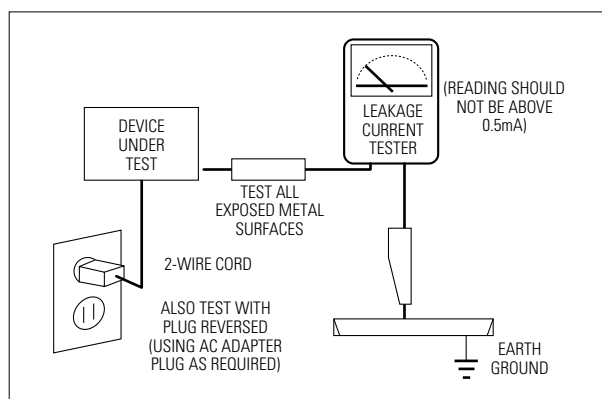


Fig. 1-1 AC Leakage Test

6. Antenna Cold Check:
With the unit's AC plug disconnected from the AC source, connect an electrical jumper across the two AC prongs. Connect one lead of the ohmmeter to an AC prong. Connect the other lead to the coaxial connector.
7. High Voltage Limits:
High voltage must be measured each time servicing is done on the B+, horizontal deflection or high voltage circuits.



1-2 Safety Precautions (Continued)

8. High voltage is maintained within specified limits by close-tolerance, safety-related components and adjustments. If the high voltage exceeds the specified limits, check each of the special components.
9. Design Alteration Warning:
Never alter or add to the mechanical or electrical design of this unit. Example: Do not add auxiliary audio or video connectors. Such alterations might create a safety hazard. Also, any design changes or additions will void the manufacturer's warranty.
10. Hot Chassis Warning:
Some TV receiver chassis are electrically connected directly to one conductor of the AC power cord. If an isolation transformer is not used, these units may be safely serviced only if the AC power plug is inserted so that the chassis is connected to the ground side of the AC source.

To confirm that the AC power plug is inserted correctly, do the following: Using an AC voltmeter, measure the voltage between the chassis and a known earth ground. If the reading is greater than 1.0V, remove the AC power plug, reverse its polarity and reinsert. Re-measure the voltage between the chassis and ground.
11. Some TV chassis are designed to operate with 85 volts AC between chassis and ground, regardless of the AC plug polarity. These units can be safely serviced only if an isolation transformer inserted between the receiver and the power source.
12. Some TV chassis have a secondary ground system in addition to the main chassis ground. This secondary ground system is not isolated from the AC power line. The two ground systems are electrically separated by insulating material that must not be defeated or altered.
13. Components, parts and wiring that appear to have overheated or that are otherwise damaged should be replaced with parts that meet the original specifications. Always determine the cause of damage or overheating, and correct any potential hazards.
14. Observe the original lead dress, especially near the following areas: Antenna wiring, sharp edges, and especially the AC and high

voltage power supplies. Always inspect for pinched, out-of-place, or frayed wiring. Do not change the spacing between components and the printed circuit board. Check the AC power cord for damage. Make sure that leads and components do not touch thermally hot parts.

15. Product Safety Notice:
Some electrical and mechanical parts have special safety-related characteristics which might not be obvious from visual inspection. These safety features and the protection they give might be lost if the replacement component differs from the original—even if the replacement is rated for higher voltage, wattage, etc.

Components that are critical for safety are indicated in the circuit diagram by shading, () or ()

Use replacement components that have the same ratings, especially for flame resistance and dielectric strength specifications. A replacement part that does not have the same safety characteristics as the original might create shock, fire or other hazards.

1-3 Servicing Precautions

Warning 1 : First read the "Safety Precautions" section of this manual. If some unforeseen circumstance creates a conflict between the servicing and safety precautions, always follow the safety precautions.

Warning 2 : An electrolytic capacitor installed with the wrong polarity might explode.

1. Servicing precautions are printed on the cabinet. Follow them.
2. Always unplug the unit's AC power cord from the AC power source before attempting to: (a) Remove or reinstall any component or assembly, (b) Disconnect an electrical plug or connector, (c) Connect a test component in parallel with an electrolytic capacitor.
3. Some components are raised above the printed circuit board for safety. An insulation tube or tape is sometimes used. The internal wiring is sometimes clamped to prevent contact with thermally hot components. Reinstall all such elements to their original position.
4. After servicing, always check that the screws, components and wiring have been correctly reinstalled. Make sure that the portion around the serviced part has not been damaged.
5. Check the insulation between the blades of the AC plug and accessible conductive parts (examples: metal panels, input terminals and earphone jacks).
6. Never defeat any of the B+ voltage interlocks. Do not apply AC power to the unit (or any of its assemblies) unless all solid-state heat sinks are correctly installed.
7. Always connect a test instrument's ground lead to the instrument chassis ground before connecting the positive lead; always remove the instrument's ground lead last.
8. Plasma display panels have partial afterimages when a same picture continues to be displayed for a certain time. This happens due to the degradation of brightness caused by a scale-down effect.
To prevent such afterimages when displaying a same picture for a certain time, be sure to reduce the level of brightness and contrast.
ex) Contrast : 50 or 75, Brightness : 25
9. Plasma display is an array of pixels(cells). Therefore, if at least 99.9% pixels keep normal, the appropriate panel is judged as 'approved product.' Even though some of pixels keep luminescent or always light off, do not worry because the panel is approved.

1-4 Precautions for Electrostatically Sensitive Devices (ESDs)

1. Some semiconductor (“solid state”) devices are easily damaged by static electricity. Such components are called Electrostatically Sensitive Devices (ESDs); examples include integrated circuits and some field-effect transistors. The following techniques will reduce the occurrence of component damage caused by static electricity.
2. Immediately before handling any semiconductor components or assemblies, drain the electrostatic charge from your body by touching a known earth ground. Alternatively, wear a discharging wrist-strap device. (Be sure to remove it prior to applying power—this is an electric shock precaution.)
3. After removing an ESD-equipped assembly, place it on a conductive surface such as aluminum foil to prevent accumulation of electrostatic charge.
4. Do not use freon-propelled chemicals. These can generate electrical charges that damage ESDs.
5. Use only a grounded-tip soldering iron when soldering or unsoldering ESDs.
6. Use only an anti-static solder removal device. Many solder removal devices are not rated as “anti-static”; these can accumulate sufficient electrical charge to damage ESDs.
7. Do not remove a replacement ESD from its protective package until you are ready to install it. Most replacement ESDs are packaged with leads that are electrically shorted together by conductive foam, aluminum foil or other conductive materials.
8. Immediately before removing the protective material from the leads of a replacement ESD, touch the protective material to the chassis or circuit assembly into which the device will be installed.
9. Minimize body motions when handling unpackaged replacement ESDs. Motions such as brushing clothes together, or lifting a foot from a carpeted floor can generate enough static electricity to damage an ESD.

CAUTION

These servicing instructions are for use by qualified service personnel only. To reduce the risk of electric shock do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so.

2. Reference Information

2-1 Tables of Abbreviations and Acronyms

Table 2-1 Abbreviations

A	Ampere	MV	Megavolt
Ah	Ampere-hour	MW	Megawatt
Å	Angstrom	MΩ	Megohm
dB	Decibel	m	Meter
dBm	Decibel Referenced to One Milliwatt	μA	Microampere
°C	Degree Celsius	μF	Microfarad
°F	Degree Fahrenheit	μH	Microhenry
°K	degree Kelvin	μm	Micrometer
F	Farad	μs	Microsecond
G	Gauss	μW	Microwatt
GHz	Gigahertz	mA	Milliampere
g	Gram	mg	Milligram
H	Henry	mH	Millihenry
Hz	Hertz	ml	Milliliter
h	Hour	mm	Millimeter
ips	Inches Per Second	ms	Millisecond
kWh	Kilowatt-hour	mV	Millivolt
kg	Kilogram	nF	Nanofarad
kHz	Kilohertz	Ω	Ohm
kΩ	Kilohm	pF	Picofarad
km	Kilometer	lb	Pound
km/h	Kilometer Per Hour	rpm	Revolutions Per Minute
kV	Kilovolt	rps	Revolutions Per Second
kVA	Kilovolt-ampere	s	Second (Time)
kW	Kilowatt	V	Volt
l	Liter	VA	Volt-ampere
MHz	Megahertz	W	Watt
		Wh	Watt-hour

Table 2-2 Table of Acronyms

ABL	Automatic Brightness Limiter	I/O	Input/output
AC	Alternating Current	L	Left
ACC	Automatic Chroma Control	L	Low
AF	Audio Frequency	LED	Light Emitting Diode
AFC	Automatic Frequency Control	LF	Low Frequency
AFT	Automatic Fine Tuning	MOSFET	Metal-Oxide-Semiconductor-Field-Effect-Tr
AGC	Automatic Gain Control	MTS	Multi-channel Television Sound
AM	Amplitude Modulation	NAB	National Association of Broadcasters
ANSI	American National Standards Institute	NEC	National Electric Code
APC	Automatic Phase Control	NTSC	National Television Systems Committee
APC	Automatic Picture Control	OSD	On Screen Display
A/V	Audio-Video	PCB	Printed Circuit Board
AVC	Automatic Volume Control	PLL	Phase-Locked Loop
BAL	Balance	PWM	Pulse Width Modulation
BPF	Bandpass Filter	QIF	Quadrature Intermediate Frequency
B-Y	Blue-Y	R	Right
CATV	Community Antenna Television (Cable TV)	RC	Resistor & Capacitor
CB	Citizens Band	RF	Radio Frequency
CCD	Charge Coupled Device	R-Y	Red-Y
CCTV	Closed Circuit Television	SAP	Second Audio Program
Ch	Channel	SAW	Surface Acoustic Wave(Filter)
CRT	Cathode Ray Tube	SIF	Sound Intermediate Frequency
CW	Continuous Wave	SMPS	Switching Mode Power Supply
DC	Direct Current	S/N	Signal/Noise
DVM	Digital Volt Meter	SW	Switch
EIA	Electronics Industries Association	TP	Test Point
ESD	Electrostatic Discharge	TTL	Transistor Transistor Logic
ESD	Electrostatically Sensitive Device	TV	Television
FBP	Feedback Pulse	UHF	Ultra High Frequency
FBT	Flyback Transformer	UL	Underwriters Laboratories
FF	Flip-Flop	UV	Ultraviolet
FM	Frequency Modulation	VCD	Variable-Capacitance Diode
FS	Fail Safe	VCO	Voltage Controlled Oscillator
GND	Ground	VCXO	Voltage Controlled Crystal Oscillator
G-Y	Green-Y	VHF	Very High Frequency
H	High	VIF	Video Intermediate Frequency
HF	High-Frequency	VR	Variable Resistor
HI-FI	High Fidelity	VTR	Video Tape Recorder
IC	Inductance-Capacitance	VTVM	Vacuum Tube Voltmeter
IC	Integrated Circuit	TR	Transistor
IF	Intermediate Frequency		

3. Specifications

3-1 Display(PDP Monitor)

MODEL		PPM42S2
Dimensions (mm/inch)	Display	1038.8(W) x 89(D) x 635(H)mm / 40.9(W) x 3.5(D) x 25(H) Inches
	Remote Control	54(W) x 31.5(D) x 220(H)mm / 2.13(W) x 1.24(D) x 8.66(H) Inches
Weight	Display	32Kg / 70.55 lbs
	Remote Control	150g (Including batteries) / 0.33 lbs
Voltage		AC 100-240V, 50/60Hz
Power Consumption		310 Watts
Number of Pixels		852(H) X 480(V)
Screen Size		106Cm / 42 Inches
AUDIO Input		VIDEO / S-VIDEO COMPONENT PC (RGB)
AUDIO Output		7W + 7W (8Ω)
VIDEO Input		VIDEO S-VIDEO COMPONENT 1(480i) / 2 (480p/720p/1080i) PC (RGB 1 : D-SUB / RGB 2 : BNC)

MENO

4. Alignment and Adjustments

4-1 Service Mode

4-1-1 SERVICE MODE ENTRY METHOD (General Transmitter)

1. Turn off the power to make the SET STAND-BY mode.
2. In order to enter the Service Mode, select MUTE-1-8-2-POWER.

* In case entry into SERVICE MODE is unsuccessful, repeat the procedures above.

4-1-2 Initial DISPLAY State in times of SERVICE MODE Switch overs

4-1-2(A) OSD DISPLAY

MENU	
1. PWS364	9. Pinp Control
2. VPC3230	10.OSD Position
3. SDA9400	11. Test Pattern
4. SDA9280	12. Option Table
5. AD9884 - Video	13.Reset
6. AD9884 - DTV/PC	
7. CXA2101Q-1	
8. CXA2101Q-2	
Release Time :	

4-1-2(B) BUTTONS OPERATIONS WITHIN SERVICE MODE

Menu	Entire menu display
Joystick UP/DOWN	Cursor move to select items
Joystick (LEFT/RIGHT)	Enable to increase and decrease the data of the selected items

4-1-3 Details of Control

4-1-3(A) PW364

No	OSD	Default of MODE			
		VIDEO / S-VHS	Component1	Component2	PC
1	H Position	30	-	27	93
2	V Position	34	-	20	35
3	Red Gain	148	-	125	113
4	Green Gain	148	-	125	113
5	Blue Gain	148	-	125	113
6	Red Offset	133	-	129	139
7	Green Offset	133	-	129	139
8	Blue Offset	133	-	129	139
9	APL On/Off	1	-	1	1
10	High Light	148	-	125	113
11	Low Light	133	-	129	139
12	Shit Pixel	on	-	on	on
13	Test	0	-	0	0
14	Pixel Number	4	-	4	4
15	Shift Line	4	-	4	4
16	Time	4	-	4	4

4-1-3(B) VPC3230

No	OSD	Default of MODE			
		VIDEO / S-VHS	Component1	Component2	PC
1	Bright YUV	195	-	195	DO NOT ENTER
2	Cont YUV	27	-	27	
3	IF Comp(IFC)	2	-	2	
4	Chroma band(CBW)	3	-	3	
5	Ena Luma	1	-	1	
6	HPLL Speed	1	-	1	
7	Luma Delay	4	-	4	
8	3230 Bright	146	-	146	
9	3230 Contrast	45	-	45	
10	H LPF Y/C(LPF2)	0	-	0	
11	H LPF Chroma(CBW2)	0	-	0	
12	H Peaking (Filter)	2	-	1	
13	Coaring Off/On	1	-	1	
14	PK	3	-	3	

4-1-3(C) SDA9400

No	OSD	Default of MODE			
		VIDEO / S-VHS	Component1	Component2	PC
1	SNR On	1	-	-	DO NOT ENTER
2	VCSNR On	1	-	-	
3	HCSNR On	0	-	-	
4	DTNR On	1	-	-	
5	TNRCLY	5	-	-	
6	TNRCNC	5	-	-	

Alignment and Adjustments

4-1-3(D) SDA9280

No	OSD	Default of MODE			
		VIDEO / S-VHS	Component1	Component2	PC
1	CTI Thresh	0	-	-	DO NOT ENTER
2	CTI Trawid	0	-	-	
3	Y-Delay	11	-	-	
4	LPF Gain	7	-	-	
5	BPF Gain	11	-	-	
6	HPF Gain	12	-	-	
7	Phacom	2	-	-	
8	Cor	1	-	-	

4-1-3(E) AD9884

No	OSD	Default of MODE			
		VIDEO / S-VHS	Component1	Component2	PC
1	Red Gain	143	-	142	145
2	Green Gain(Fix)	132	-	132	132
3	Blue Gain	143	-	143	137
4	Red Offset	38	-	28	34
5	Green Offset(Fix)	32	-	32	32
6	Blue Offset	25	-	21	27
7	Current	1	-	-	-

4-1-3(F) CXA2101Q-1

No	OSD	Default of MODE			
		VIDEO / S-VHS	Component1	Component2	PC
1	Sub Bright	52	-	52	DO NOT ENTER
2	Limit Level	0	-	0	
3	System	1	-	2	
4	D-Color	1	-	1	
5	R Drive	32	-	32	
6	G Drive	32	-	32	
7	B Drive	32	-	32	
8	R Cutoff	32	-	32	
9	G Cutoff	32	-	32	
10	B Cutoff	32	-	32	
11	ABL Mode	0	-	0	
12	ABL TH	0	-	0	
13	H sep sel	0	-	0	
14	Fix Sync	0	-	0	
15	V Time Con	1	-	1	
16	H Width	1	-	1	
17	HHD Time Con	0	-	0	
18	Picture	10	-	10	

Alignment and Adjustments

4-1-3(G) CXA2101Q-2

No	OSD	Default of MODE			
		VIDEO / S-VHS	Component1	Component2	PC
1	HS Mask	1	-	1	DO NOT ENTER
2	Sub Cont	8	-	7	
3	Sub Color	14	-	14	
4	Sub Hue	5	-	6	
5	Sub SHP	2	-	2	
6	R-Y/R	7	-	7	
7	R-Y/B	14	-	14	
8	G-Y/R	12	-	6	
9	G-Y/B	5	-	7	
10	PABL Level	6	-	6	
11	SHP FO	2	-	2	
12	Pre/Over	0	-	0	
13	CTI Level	1	-	1	
14	LTI Level	0	-	0	
15	DC-Tran	2	-	1	
16	D-Pic	3	-	2	
17	Color	26	-	26	
18	Brightness	37	-	35	

4-1-3(H) PinP Control

No	OSD	Default of MODE			
		VIDEO / S-VHS	Component1	Component2	PC
1	Pip HPos	6	6	-	-
2	Pip VPos	13	13	-	-
3	Bright YUV	195	195	-	-
4	Cont YUV	27	27	-	-
5	Luma Delay	0	0	-	-
6	3230 Bright	40	40	-	-
7	3230 Contrast	38	38	-	-

4-1-4 White Balance Adjust Method

1. Press MUTE-1-8-2-POWER to enter the factory mode.
2. Enter "5. AD9884 - Video" or " 6. AD9884 - DTV/PC".
3. Adjust LOW coordinates as R,B OFFSET and HIGH coordinates as R,B GAIN.
(GREEN is fixed)
4. Press "Menu" Key in remote control to exit.
5. Enter "1. PW364A".
6. Adjust LOW light as "Low Light".
7. Adjust HIGH light as "High Light".

- W/B Adjustment SPEC(Suwon Factory Toshiba PATTERN)

	W/B		x	y	Y(fL)	T(K)
VIDEO (10 Gray)	Picture Quality Assessment	High (⑥)	285	295	19	9200
		Low (②)	285	295	0.7	9200
D T V (9 Gray)	Picture Quality Assessment	High (⑥)	285	295	21	9200
		Low (②)	285	295	0.95	9200
P C (16 Gray)	Picture Quality Assessment	High (⑨)	285	295	14	9200
		Low (③)	285	295	0.65	9200

< Condition of Signals

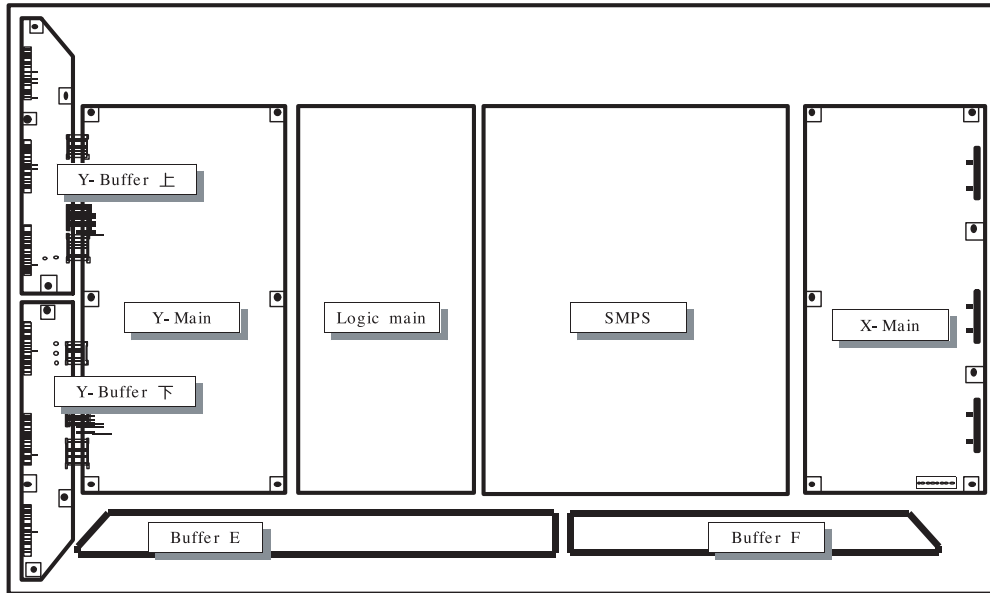
- ① Video,S-VHS, Component1(DVD) : 10-Gray: (0,1,②,3,4,5,⑥,7,8,9,10)-ShibaSoku TG71BX
- ② Component 2(DTV) : 9 Gray : (0,1,②,3,4,5,⑥,7,8,9) - LT446 1080i output
- ③ PC : 16 Gray (0,1,2,③,4,5,6,7,8,⑨,10....15) - TP36B

4-2 PPM42S2 PC Input Mode

Video Signal	Dot Line	Vertical Frequency (Hz)	Horizontal Frequency (KHz)	Vertical Polarity	Horizontal Polarity
IBM PC/AT Compatible	640 X 350	70.086	31.469	N	P
		85.080	37.861	N	P
	640 X 400	85.080	37.861	P	N
	720 X 400	70.087	31.469	P	N
		85.039	37.927	P	N
	640 X 480	59.940	31.469	N	N
		72.809	37.861	N	N
		75.000	37.500	N	N
		85.008	43.269	N	N
	848 X 480	60.000	29.800	N/P	N/P
	852 X 480	60.000	31.731	N	N
	800 X 600	56.250	35.156	N/P	N/P
		60.317	37.879	P	P
		72.188	48.077	P	P
		75.000	46.875	P	P
	1024 X 768	85.061	53.674	P	P
		60.004	48.363	N	N
		70.069	56.476	N	N
		75.029	60.023	P	P
		84.997	68.677	P	P

4-3 Discharge Voltage Adjustments When Replacing Main Assy

PDP Driving related Board Layout



Voltage Adjustments

- n Adjust all of variable resistances except V9, VG clockwise to decrease the voltage.
- n For PPM42S2 models, readjust VR (6V) to 5.9V (±0.2V).

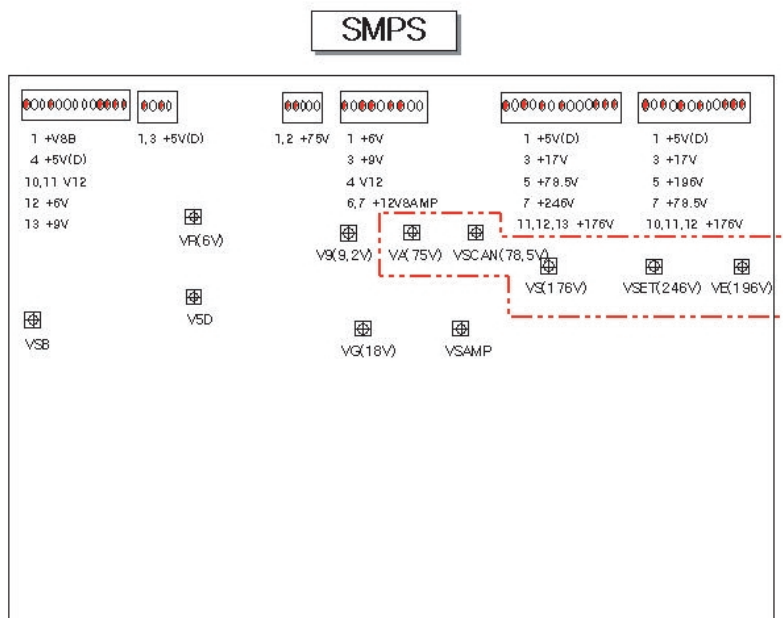


Table of Voltage Values

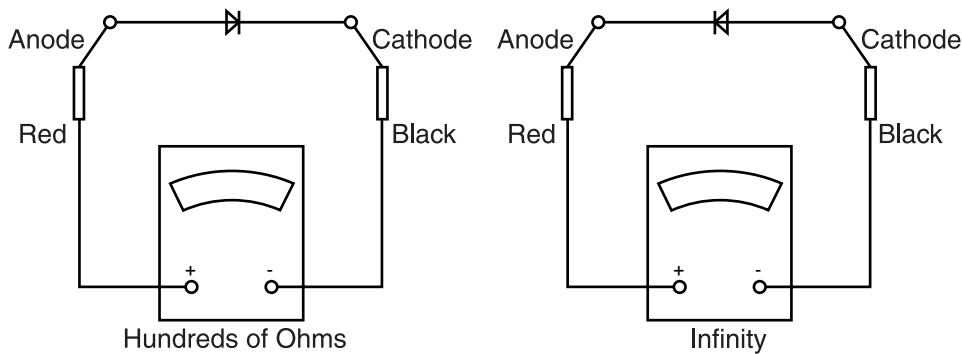
Output Voltage	Voltage Values (V)
VE	See the label attached on the module base chassis
VSET	
VS	
VSCAN	
VA	
VS AMP	12
VG	18.3
V9	9
V5D	5.3
VR(6V)	5.9
VSB	5

- n When replacing the X, Y driving boards, avoid waveform adjustments using variable resistance as they have been adjusted according to the characteristics of PDP panel.

4-4 Fault Finding Using MULTI METER

Parts defects can be found for DIODE TRANSISTOR IC, using MULTI TEST including Forward/Reverse direction Multi Test. Of course, in case resistance of several ohms and COIL are connected in parallel circuit, the lock out circuit parallel connected to part must be severed.

1. DIODE



	Forward Direction	Reverse Direction
Between Anode and Cathode	Hundreds of ohms	Infinity

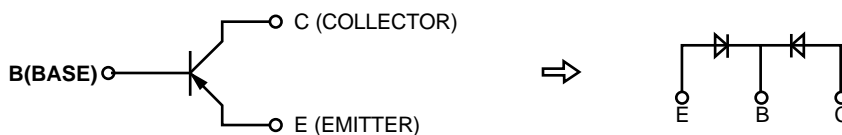
2. TRANSISTOR

1 For NPN(KSC815-Y, 2SC2068, 2SC2331-Y)



	Forward Direction	Reverse Direction
Between B and E	Hundreds of ohms	Infinity
Between B and C	Hundreds of ohms	Infinity
Between E and C	Infinity	Infinity

1 For PNP(KSA539-Y)



	Forward Direction	Reverse Direction
Between B and E	Hundreds of ohms	Infinity
Between B and C	Hundreds of ohms	Infinity
Between E and C	Infinity	Infinity

3. IC (INTEGRATED CIRCUIT)

IC has built in DIODE against overvoltage in PIN. Generally, except for internal circuit defects, IC defects can be found, by measuring the DIODE.

Forward Direction	Hundreds of ohms
Reverse Direction	Varying depending on IC but generally normal
	Infinity in DIODE TEST MODE

- > Defects have SHORT(0 ohm) for both forward and reverse direction.

5. Circuit Description

5-1 Power supply

5-1-1 Outline(PDP SMPS)

Considering various related conditions, the switching regulator with good efficiency and allowing for its small size and lightweight was used as the power supply for PDP. Most of the power supply components used forward converter, and Vsamp and Vsb used simple flyback converter.

To comply with the international harmonics standards and improve the power factor, active PFC (Power Factor Correction) was used to rectify AC input into +400V DC output, which in turns used as input to the switching regulator.

5-1-2 42"SD SMPS SPECIFICATION

5-1-2(A) INPUT

PDP-42PS board is designed so that input power can be used within AC 90 VAC to 264 VAC with 50/60Hz \pm 3Hz.

5-1-2(B) OUTPUT

PDP-42PS board provides 13 output switching power supplies (+165Vs, +220Set, +185Ve, +75Va, +80Scan, +18Vg, +5Vsb, +5V(D), +5.9V(A), +12V. +9V, +12Vfan, and +12Vsamp). The output voltage, and current requirements for continuous operation are stated below (Table 3).

Table1. Specifications of Output Power Supplies for PDP SMPS

Output Name	Output Voltage	Output Current	Using in PDP driving
Vs	+165V	1.4A	Sustain Voltage of Drive Board
Va	+75V	0.5A	Address Voltage of Drive Board
Vscan	+80V	0.05A	
Vset	+220V	0.05A	
Ve	+185V	0.05A	
Vg	+18.3V	0.3A	
Vfan	+12V	0.8A	
V9	+9V	0.3A	
V5(A)	+5.9V	1.0A	Analog IC Drive Voltage of Video Board
V5(D)	+5.3V	3.5A	IC Drive Voltage of Logic Board
Vsb	+5V	0.4	Stand-by for Remote Control
V12	+12V	1.2A	
Vsamp	+12V	1.5A	

Table 2. Specifications to Protect PDP SMPS

Division	OCP Current	OVP Voltage	Short Circuit
Vs	5A	195V	O.K
Va	2A	90V	O.K
+5V	10A	6.2V	O.K

5-1-2(C) FUNCTION OF BOARD

(1) Remote control

Using 250V/ 10A relay, the board makes remote control available.

(2) Free voltage

The board designed so that input voltage can be used within 90 VAC to 264VAC.

(3) Embedded thermal sensor

The board is equipped with thermal sensor to detect the internal temperature of the unit, and to short relay when the internal temperature is higher than specified temperature so as to shutdown the unit.

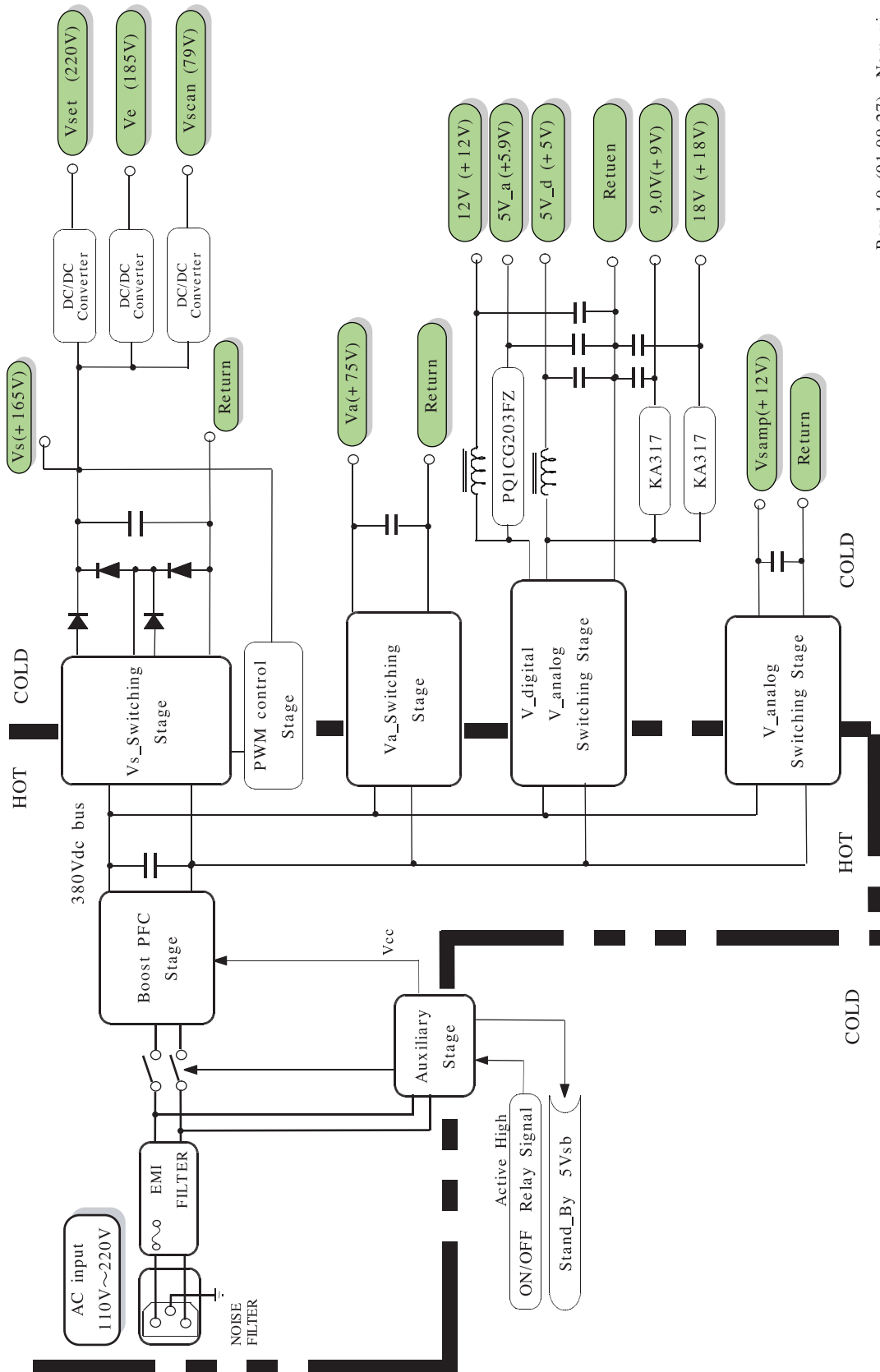
(4) Improvement of power factor

The board is designed using PFC circuit so that PF (Power Factor) can be over 0.95, because low PF can be a problem in high voltage power.

(5) Protection

The OCP (Over Current Protection), the OVP (Over voltage Protection), and the Short Circuit Protection functions are added against system malfunction.

5-1-2(D) PDP-PS-42 BLOCK DIAGRAM



Rev.1.0 (01.09.27) Nam_yi

(1) AC-DC Converter

PDP-42PS outputs +400V DC from the common AC power supply using the active PFC booster converter. This converter is designed for improving the power factor and preventing the noise with high frequency and finally becomes the input power system for the switching regulator on the output side.

(2) Auxiliary Power Supply

The auxiliary power supply is a block generating power of $\bullet\ddot{I}$ -com for remote controlling. Once the power plug is inserted, this block always comes into operation, causing $\bullet\ddot{I}$ -com to get into the stand-by state for the output. Thus, this output is called the stand-by voltage. And with the relay ON signal inputted through the remote controller, this block turns the mechanical switch of relay to ON for driving the main power supply.

(3) Implementation of Sustain Voltage

As the main part of a SMPS for PDP, sustain voltage must supply a high power, +165V/ 1.4A. It is designed using forward converter basically. At the output stage two 90V converters are connected serially for high efficiency and reduction of system size against a single 180V converter.

(4) Implementation of Small Power Output (Va, V(D), V(A), Vfan, V9, Vsamp, Ve, Vset, Vscan, V12, and Vg)Vset, Ve, and Vscan used DC-DC module. V(D), Va, V12, and Vfan used forward converter, and Vsamp used flyback converter. V(A), V9, and Vg are simply implemented using switching regulator.

5-1-3 Requirements of PDP SMPS

Since SMPS does not operate alone, but it operates with the load of the whole system, it should be designed carefully considering the load of the system. In addition, it should be designed considering emerging issues such as EMC, and protection against heat as well as system stability especially.

5-1-3(A) SAFETY AND REMOTE CONTROL CAPABILITY

Stability is one of the most important requirements for SMPS. SMPS should be designed to prevent abnormal status due to abnormal load variation so as to keep the system stable, and guarantee customer safety.

The protection circuits of SMPS include over-current protection (OCP), over voltage protection (OVP), and under voltage lock-out (UVLO), and short circuit protection circuit. Although each circuit can be implemented by various procedures, the most popular is implementing with comparator that compares current value with that of standard and determine abnormality of the circuit.

In addition, surge current protection, insulation management, and static electricity protection circuit should be added, because it uses commercial power source as an input.

PDP SMPS should be designed using auxiliary power and relay to provide remote control capability.

5-1-3(B) THE RELATION BETWEEN POWER CONSUMPTION AND POWER CONVERSION Efficiency

The power consumption and the power conversion efficiency of SMPS affect protection against heat and system operation much.

[If the power conversion efficiency of 100W SMPS is 70%, is the power loss of internal circuit 30W?]

Output power consumption P_o is determined by the multiplication of DC output voltage V_o and output current I_o . Input power consumption P_i is determined by the addition of output power consumption P_o and internal power loss of SMPS P_L .

Provided that the power conversion efficiency is η ,

$$P_i = P_o + P_L$$

$$\eta = \frac{P_o}{P_i} \quad \text{----- Equation (1)}$$

$$P_L = \left(\frac{1}{\eta} - 1\right) \cdot P_o$$

If the power conversion efficiency of 100W SMPS is 70%, the internal power loss is about 42.8W by Equation (1). If the power conversion efficiency of 400W SMPS for 42"SD is 82%, the internal power loss is 87.8W by Equation (1). Table 4 shows internal power loss as a function of output power for various power conversion efficiencies.

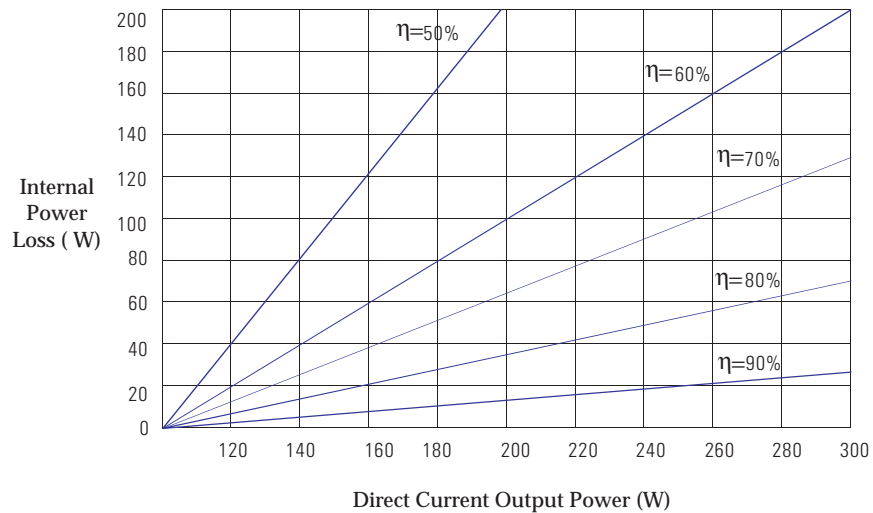


Table 4. Power Conversion Efficiency vs. Internal Power Loss

5-1-3(C) PFC (Power Factor Correction) Circuit Descriptions

The current electric devices use DC power supply and require a rectifier circuit converting AC into DC. As most rectifier circuits apply a capacitor input type, the rectifier circuit becomes the core of the occurrence of harmonics with lower reverse rate. If various electronic and electric devices are connected to a power system, high-frequency current will occur due to a power rectifier circuit, a phase control circuit with power input current of non-sine wave, or components with non-linear load characteristics, such as capacitor, inductor, etc. As the result, the disturbance of voltage occurs, and finally a power capacitor or a transformer generates heat, fire or noise occurs, controls malfunction, or the accessed devices abnormally operate or their lives are shortened. To prevent those symptoms, IEC (International Electrotechnical Commission) regulated standards for Power Supply Harmonics. (Refer to IEC 1000-3-2.) Figure 8 shows the basic structure of Active Boost PFC and waveforms.

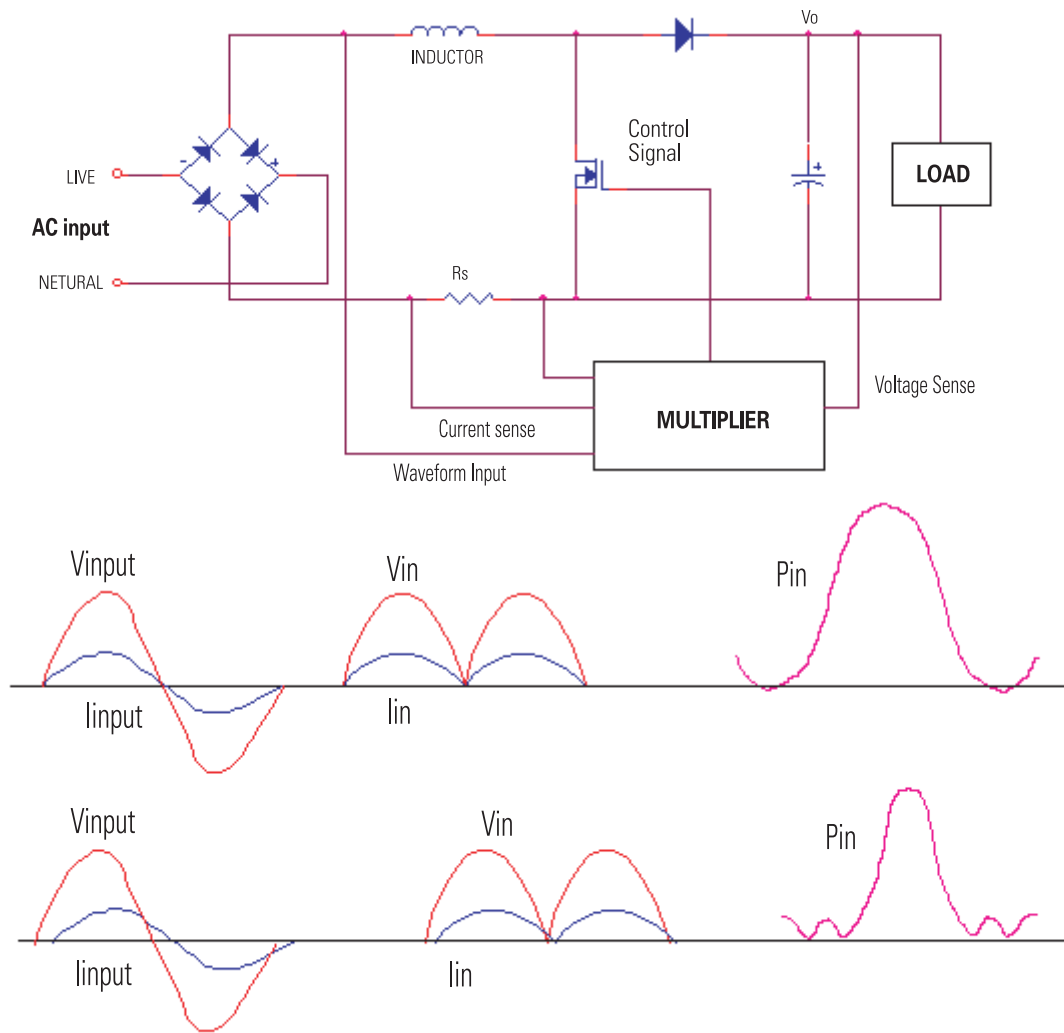
Standards for Power Supply Harmonics

Scale: Devices accessed to 220V/380V, 230V/400V, 240V/425V and lower than 16A (IEC 100-3-2)
Devices with AC 230V and lower than 16A (IEC 555-2)

Applied Classes :

- ◆ Class A : Devices not included in another class
- ◆ Class B : Portable tools
- ◆ Class C : Lighting devices
- ◆ Class D : Devices with special current waveforms

Application Schedule : Except the devices less than rating input of 75W (1996~1999)
Except the devices less than rating input of 50W (2000 and after)



The architecture and the pulse of active boost PFC

5-1-3(D) CONCLUSION

Although SMPS (Switching Mode Power Supply) enables small lightweight high-power consumption power design, it is hard to be used when stability and precise control are required. Power stage for PDP can be designed using the lightweight SMPS feature. It is important to design SMPS considering system load, stability, and related international standards.

5-2 Driver Circuit

5-2-1 Driver Circuit Overview

5-2-1(A) WHAT IS THE DEFINITION OF DRIVE CIRCUIT?

It is a circuit generating an appropriate pulse (High voltage pulse) and then driving the panel to implement images in the external terminals (X electrode group, Y electrode group and address electrode), and this high voltage switching pulse is generated by a combination of MOSFET's.

5-2-1(B) PANEL DRIVING PRINCIPLES

In PDP, images are implemented by impressing voltage on the X electrode, Y electrode and address electrode, components of each pixel on the panel, under appropriate conditions. Currently, ADS (Address & Display Separate: Driving is made by separating address and sustaining sections) is most widely used to generate the drive pulse. Discharges conducted within PDP pixels using this method can largely be classified into 3 types, as follows:

- (1) Address discharge : This functions to generate wall voltage within pixels to be lighted by addressing information to them (i.e., impressing data voltage)
- (2) Sustain discharge : This means a display section where only pixels with wall voltage by the address discharge display self-sustaining discharge by the support of such wall voltage. (Optic outputs realizing images are generated.)
- (3) Erase discharge : To have address discharge occur selectively in pixels, all pixels in the panel must have the same conditions (i.e., the same state of wall and space electric discharges). The ramp reset discharge section, therefore, is important to secure the drive margin, and methods most widely used to date include wall voltage controlling by ramp pulse.

5-2-1(C) TYPES AND DETAILED EXPLANATION OF DRIVE DISCHARGES

(1) Sustaining discharge

Sustaining discharge means a self-sustaining discharge generated by the total of the sustaining pulse voltage (usually, 160~170V) alternately given to X and Y electrodes during the sustaining period and the wall voltage that varies depending upon pixels' previous discharge status. It is operated by the memory function (through this, the current status is defined by previous operation conditions) AC PDP basically possesses. That is, when there is existing wall voltage in pixels (in other words, when pixels remain ON), the total of wall voltage and a sustaining voltage to be impressed subsequently impresses a voltage equal to or above the discharge start voltage, thereby generating discharge again, but when there is no existing wall voltage in pixels (in other words, when pixels remain OFF), the sustaining voltage only does not reach the discharge start voltage, thus causing no discharge. The sustaining discharge is a section generating actual optic outputs used in displaying images.

(2) Address discharge

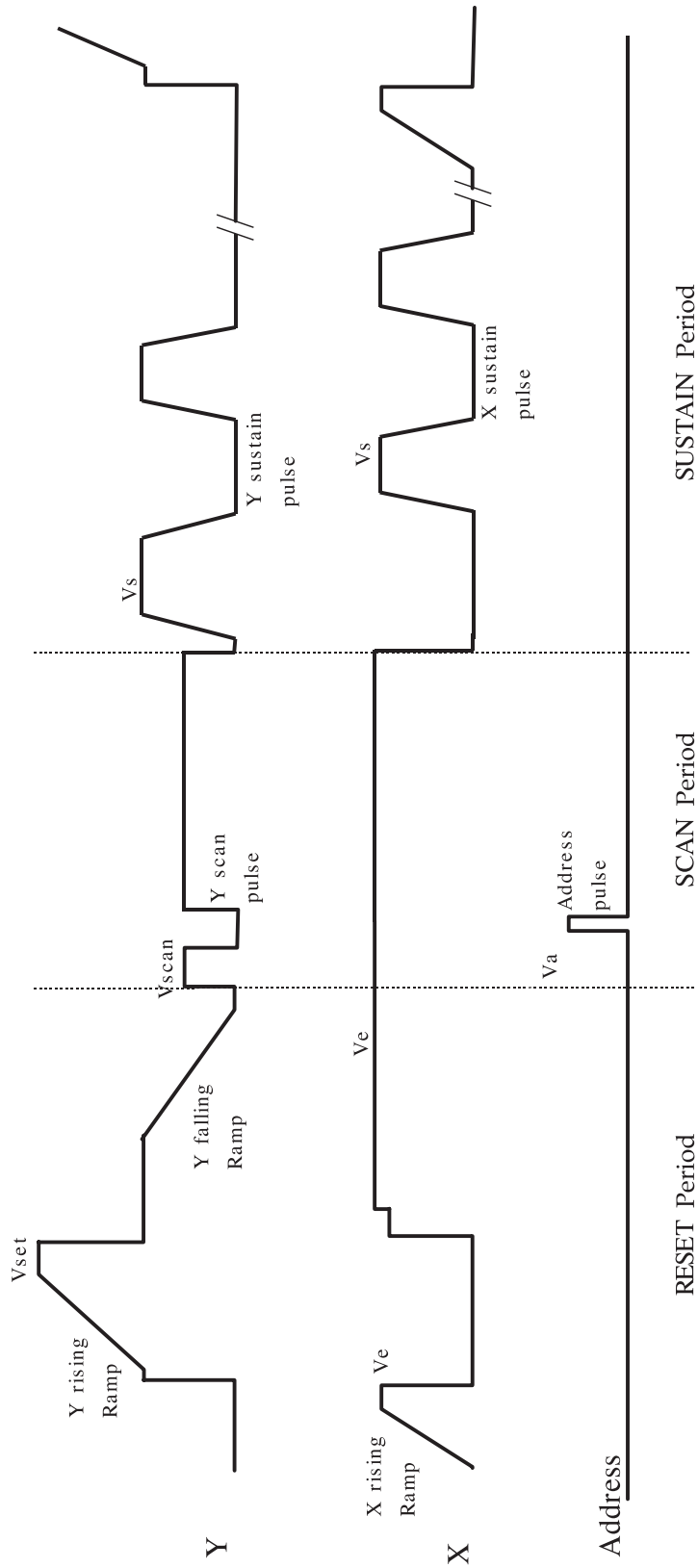
This means a discharge type generated by the difference between positive voltage of the address electrode (normally 70~75V determined by supplied V_a voltage + positive wall charge) and the negative potential of Y electrode (supplied GND level voltage + negative wall charge). The address discharge serves to generate wall voltage in pixels where images are to be displayed (that is, discharge is to be generated) prior to the sustaining discharge section. Namely, pixels with wall voltage by the address discharge will generate sustaining discharge by the following sustaining pulses.

(3) Erase discharge

The purpose of resetting or erase discharge is to make even wall voltage in all pixels on the panel. Wall voltage, which may vary depending upon the previous sustaining discharge status, must be made even. That is, wall voltage generated by the sustaining discharge must surely be removed, by making discharges and then supplying ions or electrons. Wall voltage can be removed by making discharges and then setting a limitation on time for opposite polarity charging of the wall voltage or generating weak discharge (Low voltage erasing) to supply an appropriate quantity of ions or electrons and keep polarities from being charged oppositely. The weak discharge (Low voltage erasing) methods, which have been known to date, can largely be into two types: 1) the log pulse adopted by most companies including F Company, and 2) the ramp pulse adopted by Matsushita. In both two methods, impression is made with a slow rising slope of the erasing pulse. Because the total of the existing wall voltage and a voltage on the rising pulse must be at least the drive start voltage to generate discharges, external impressed voltage is adjusted based on the difference in wall voltage between pixels. And, weak discharge is generated because of a small impressed voltage.

5-2-2 SPECIFICATION OF DRIVE PULSES

5-2-2(A) DRIVE PULSES



Al, 2,	Address (=Data) Electrode
X	Common & Sustain Electrode
Y1, 2,	Scan & Sustain Electrode

Vs	160~170V	Ve	190V~200V
Vset	210~225V	Va	70~75V
Vscan	70~75V		

5-2-2(B) FUNCTIONS OF PULSES

(1) X rising ramp pulse

Just before X rising ramp pulse is impressed, the last Y electrode sustain pulse of previous sub field is impressed. The pulse causes sustain discharge. Consequently, positive wall charge is accumulated in X electrode, and negative wall charge is accumulated in Y electrode. X rising ramp erases wall charge produced by the last sustain discharge pulse using weak-discharge.

(2) Y rising ramp pulse

During Y rising ramp period, weak-discharge begins when external voltage of about 390V~400V is impressed to Y electrode, and each gap voltage is equal to discharge start voltage. Sustaining the weak-discharge, positive wall charge is accumulated in X electrode and address electrode, and negative wall charge is accumulated in Y electrode of the entire panel.

(3) Y falling ramp pulse

During Y falling ramp period, the negative wall charge in Y electrode accumulated by 200V of X bias is used to erase positive wall charge in X electrode. Address electrode (0V) sustains most of the positive electric charge accumulated during rising ramp period so that it can maintain wall charge distribution beneficial to the upcoming address discharge.

(4) Y scan pulse

This is called the scan pulse, selecting each of Y electrodes on a one-line-at-a-time basis. In this case, V_{scan} means the scan bias voltage. About 70 V (V_{scan}) voltage is impressed on the selected electrode lines, while 0 V (GND) voltage is impressed on the other lines.

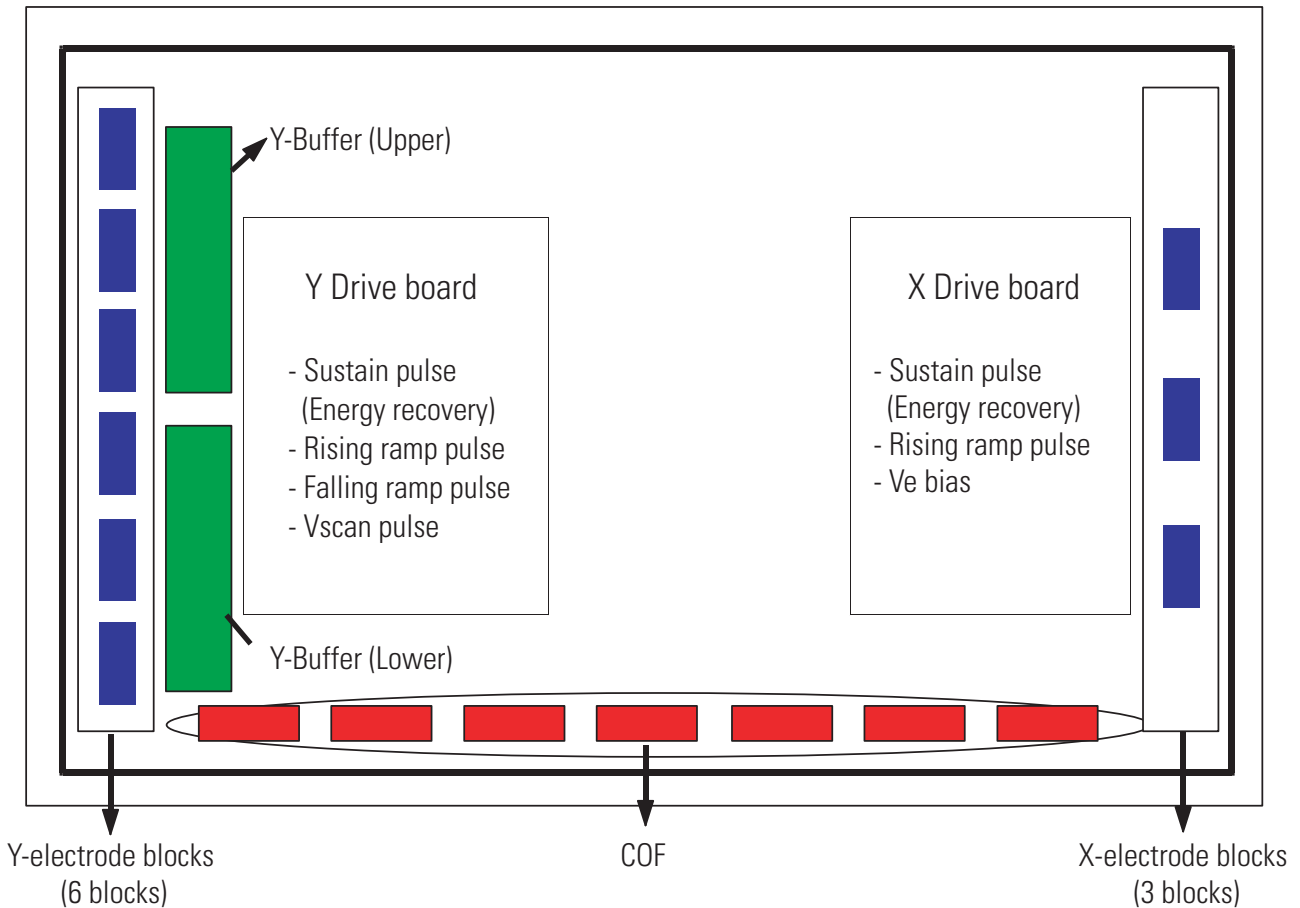
In the cells the address pulse (70V~75V) is impressed on, address discharge is occurred because negative wall charge is accumulated in Y electrode, positive wall charge is accumulated in address electrode by the applied ramp pulse, and the sum of impressed voltage is greater than discharge start voltage. Thus, because scan pulse and data pulse are impressed line by line, very long time is taken for PDP addressing.

(5) 1st sustain pulse

The sustaining pulse always begins with the Y electrode. This is because when address discharge is generated, positive wall voltage is generated on the Y electrodes. Because wall electric charge generated by address discharge is generally smaller than wall voltage generated by sustaining discharge, initial discharges have small discharge strength, and stabilization is usually obtained after 5~6 times discharges, subject to variations depending on the structure and environment of electrodes. The purpose of impressing the initial sustaining pulses long is to obtain stable initial discharges and generate wall electric charges as much as possible.

5-2-3 Configuration and Operation Principles of Driver Circuit

5-2-3(A) FUNCTIONS OF EACH BOARD



(1) X board

X board is connected to the panel's X-electrode blocks, 1) generates sustain voltage pulse (including ERC), 2) generates X rising ramp pulse, and 3) sustains V_e bias during scan period.

(2) Y board

Y board is connected to the Y-electrode blocks of panel, 1) generates sustain voltage pulse (including ERC), 2) generates Y rising and falling ramp pulse, and 3) sustains V_{scan} bias.

(3) Y buffer board (upper and lower)

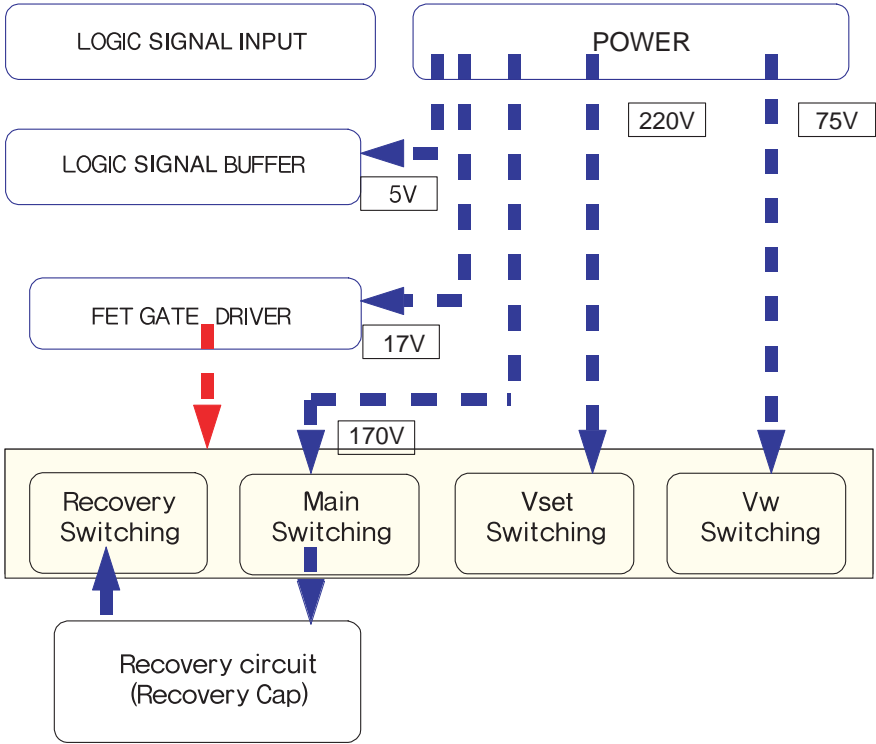
Y buffer board impresses scan pulse to Y electrodes, and consists of upper and lower sub-boards. In case of SD class, one board is equipped with 4 scan driver IC's (STMicroelectronics STV7617 with 64 or 65 outputs).

(4) COF

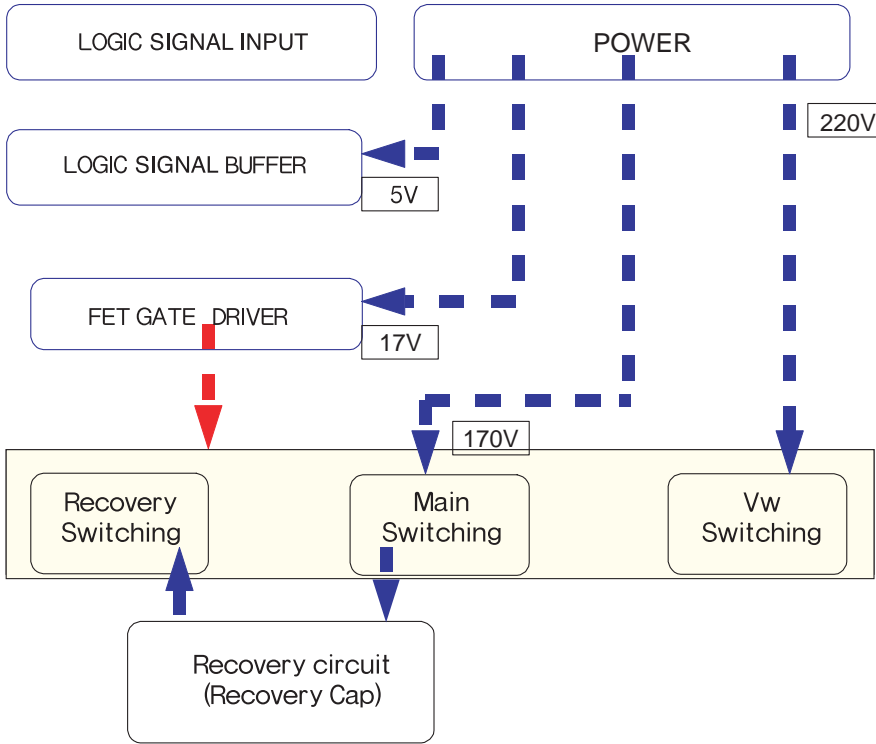
Impresses V_a pulse on address electrodes in the address section and generates address discharge based on a difference between such V_a pulse and scan pulse impressed on Y electrodes. It is in the form of COF, and a COF is equipped with 4 data drive IC's (STMicroelectronics STV7610A with 96 outputs). For a single scan, 7 COF's are required.

5-2-3(B) DRIVING BOARD'S BLOCK DIAGRAM

(1) Y



(2) X



4 Components of driving board's operations

1. Power supply

1) Supplied from the power supply board

- For sustaining discharge: 180V;
- For logic signaling buffer: 5V; and
- For gate driver IC: 15V.

2) Generated by the internal DC/DC part

- For generating V_w pulse: 180V.

2. Logic signal

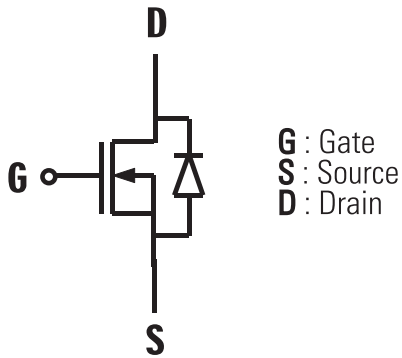
1) Supplied from the logic board

- Gate signals for FETs.

5-2-3(C) PRINCIPLES OF FET'S OPERATION AND HIGH VOLTAGE SWITCHING

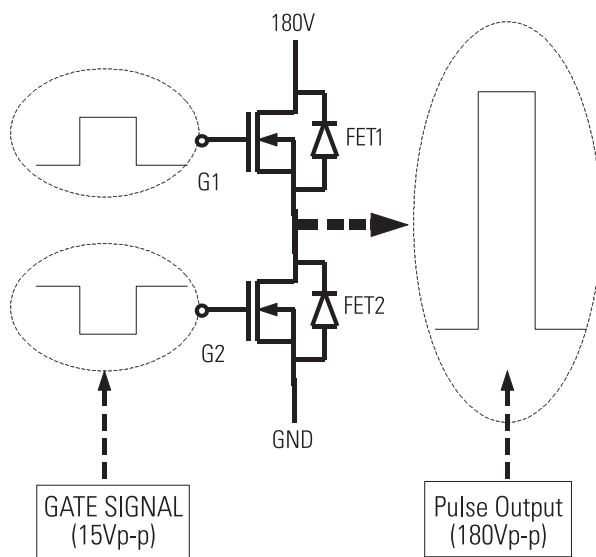
u FET's operation principles

■ FET's operation principles



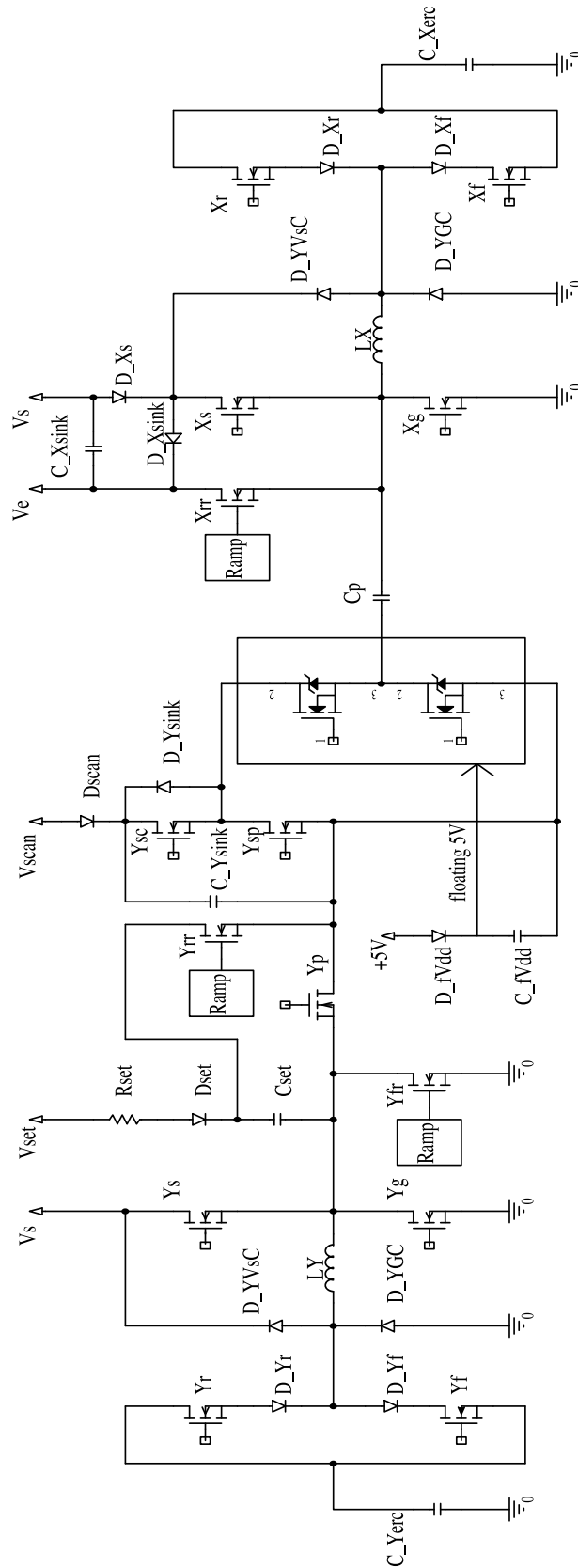
- (1) With signal impressed on the gate (Positive voltage), FET gets short-circuited (a conducting wire of zero (0) resistance); and
- (2) With no signal impressed on the gate (GND), FET gets open-circuited (a non-conducting wire of ∞ resistance).

u FET's high voltage switching principles

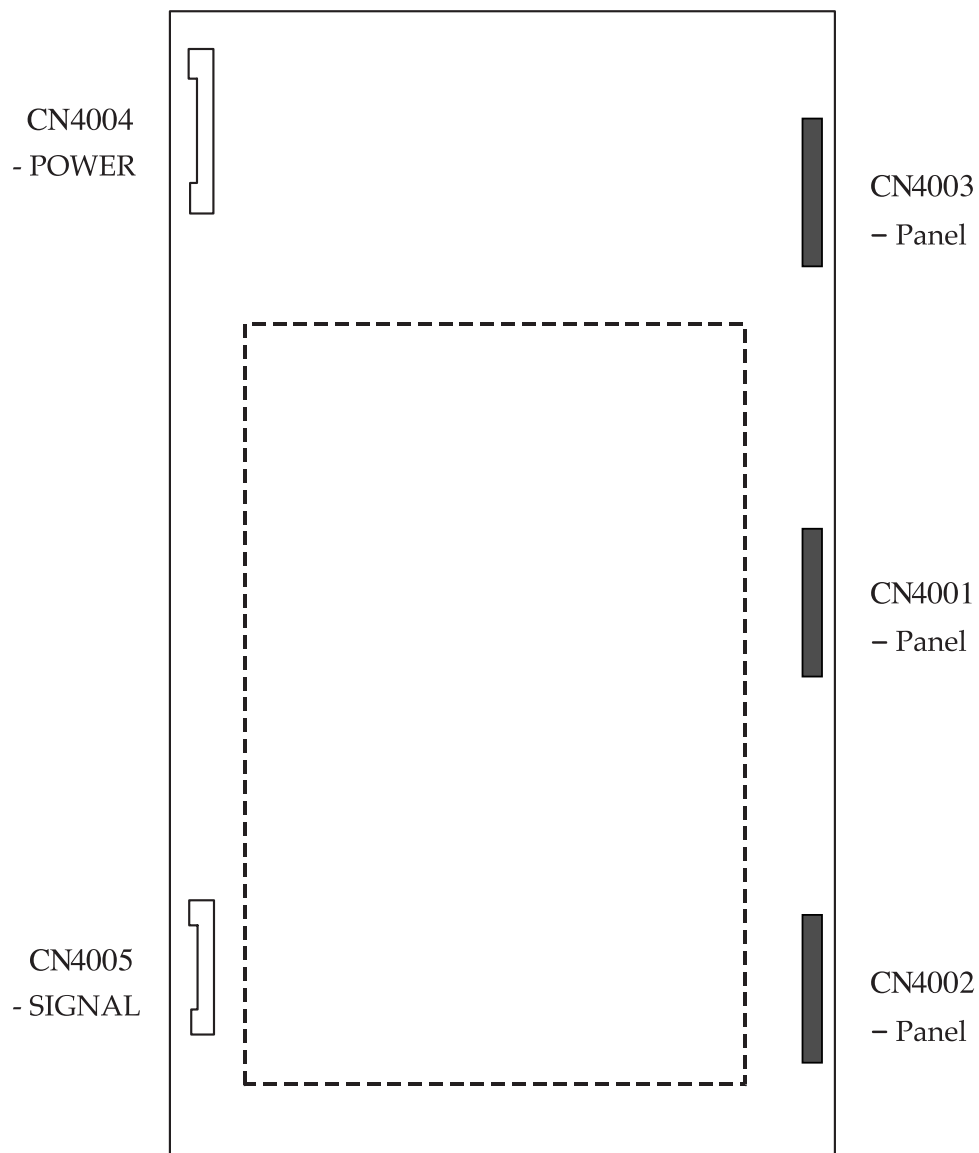


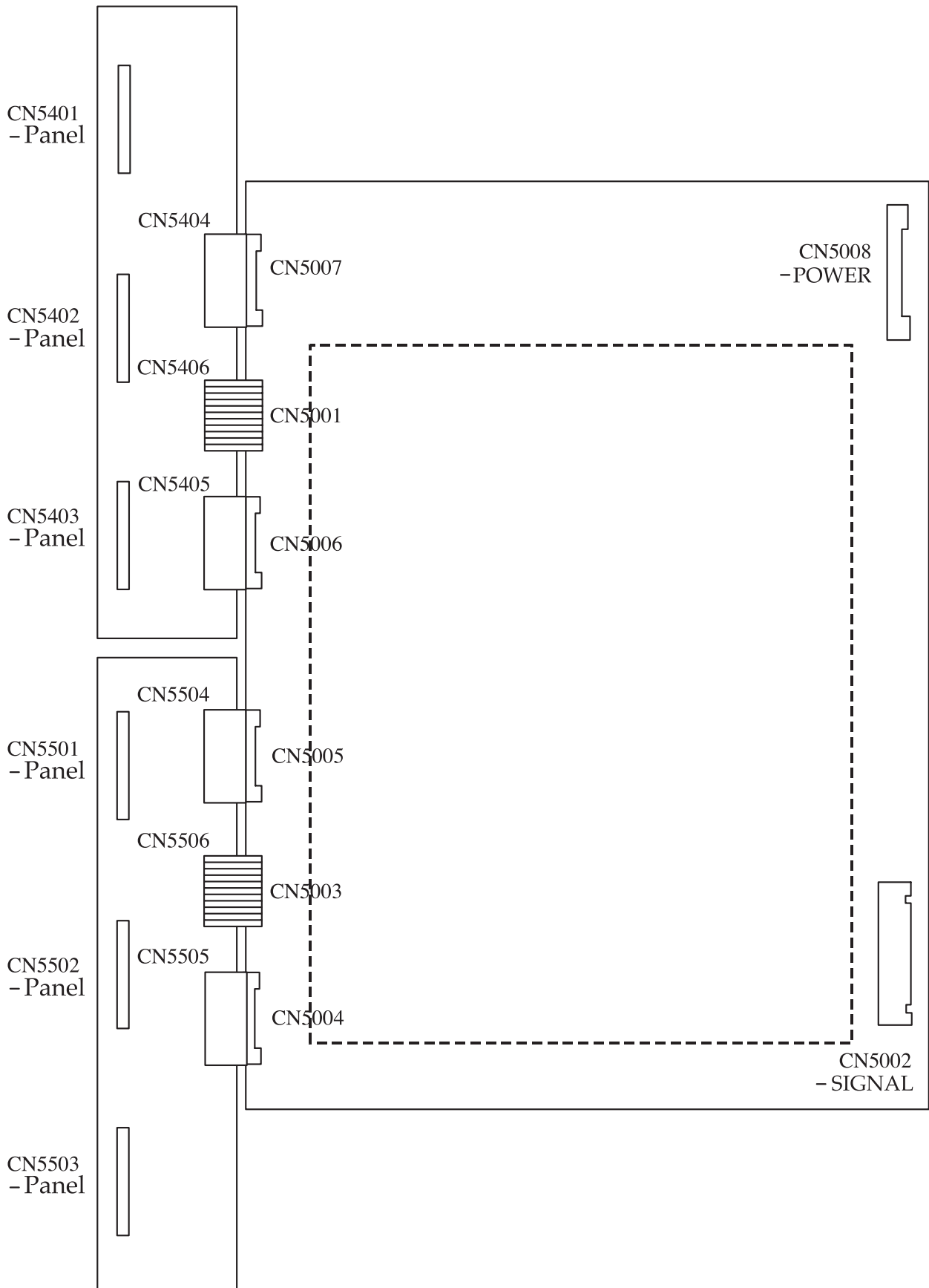
- (1) With no signal impressed on G1, FET1 gets open-circuited, and with signal impressed on G2, FET2 gets short-circuited, thereby causing GND to be outputted to output terminals.
- (2) With signal impressed on G1, FET1 gets short-circuited, and with no signal impressed on G2, FET2 gets open-circuited, thereby causing 180V to be outputted to output terminals.

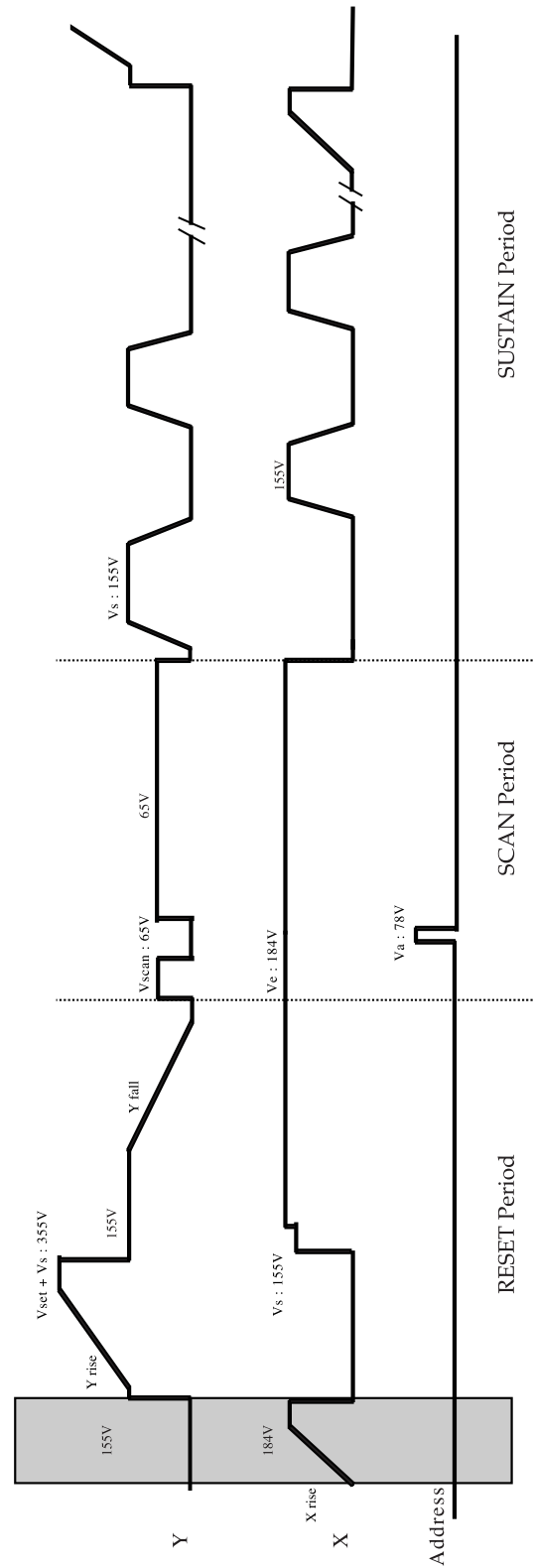
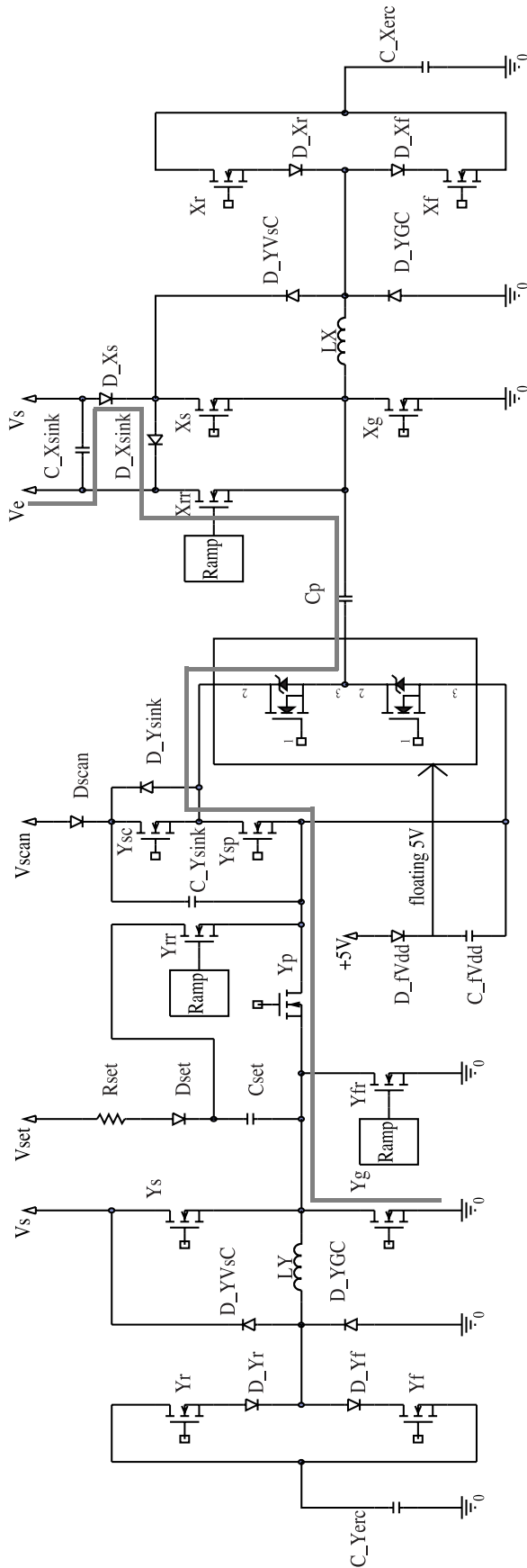
5-2-3 (D) DRIVER CIRCUIT DIAGRAM

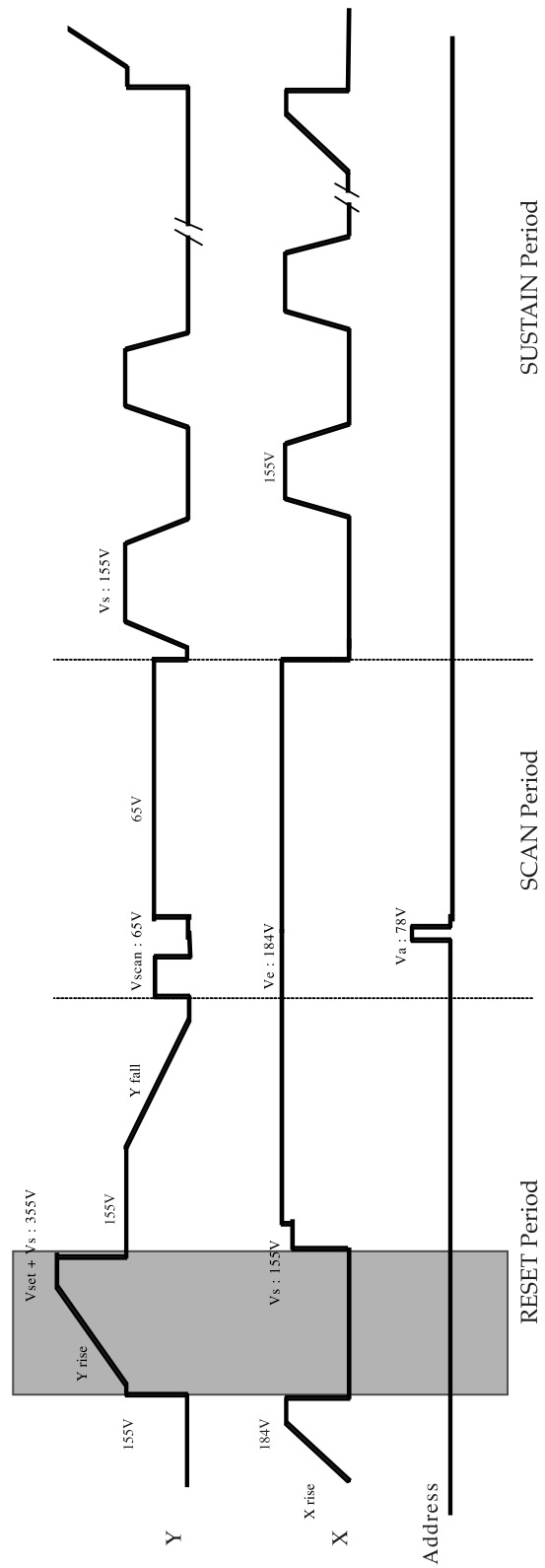
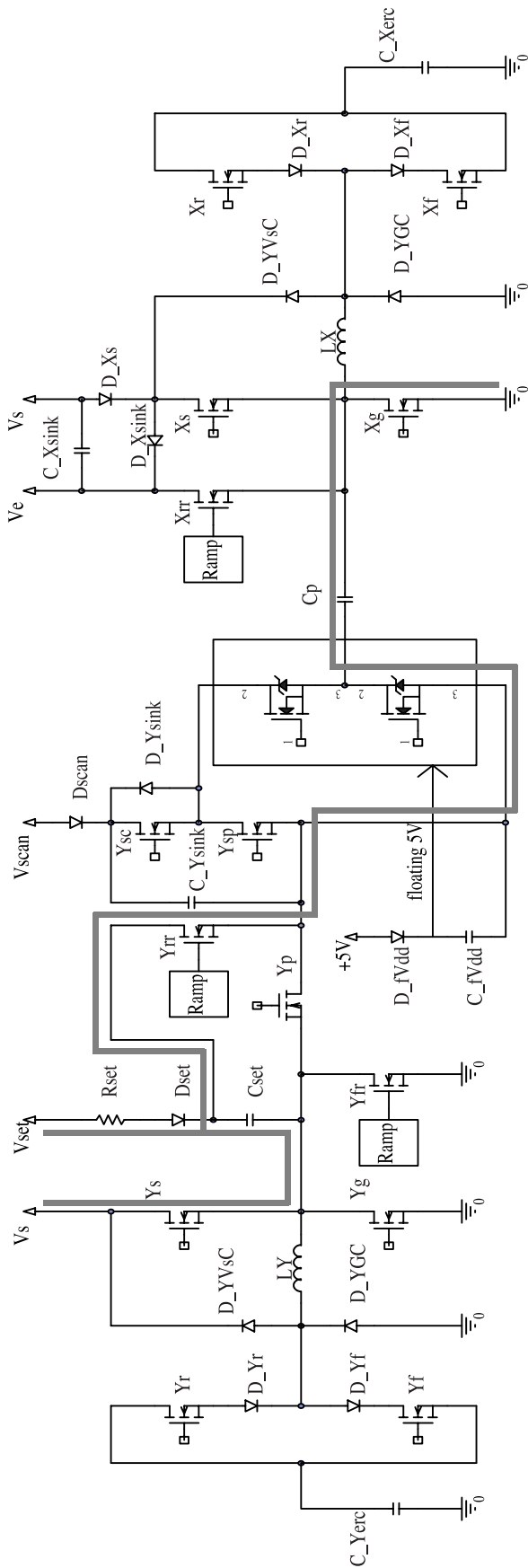


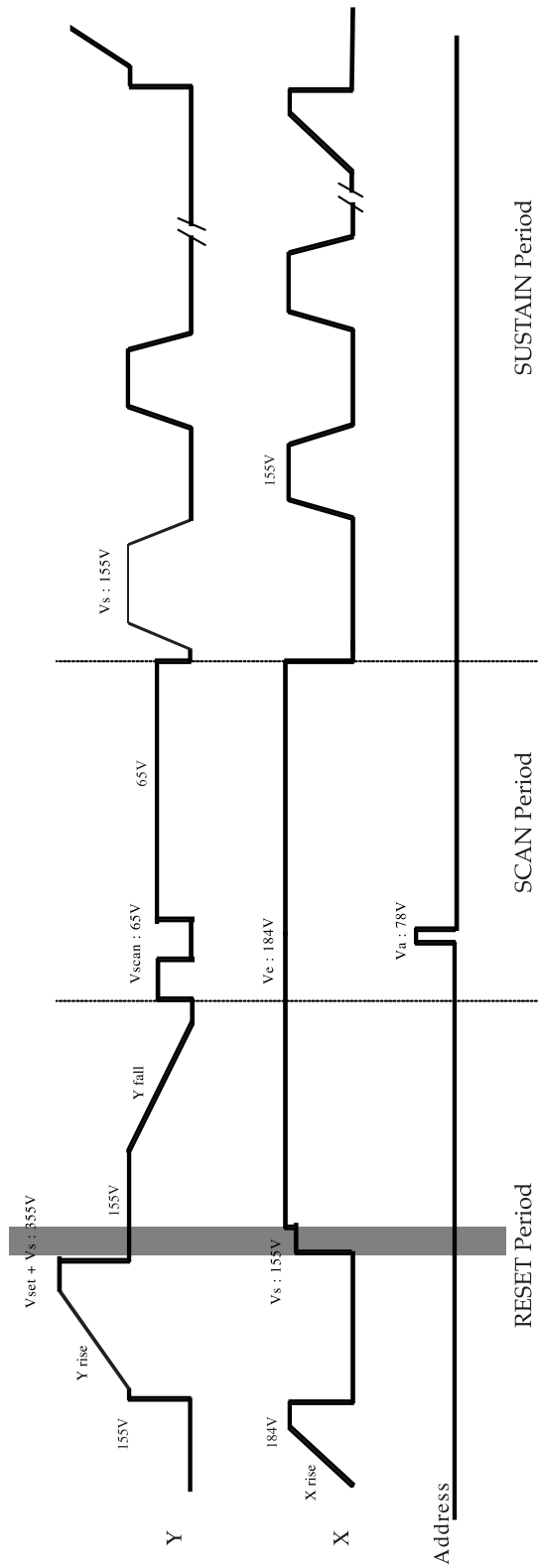
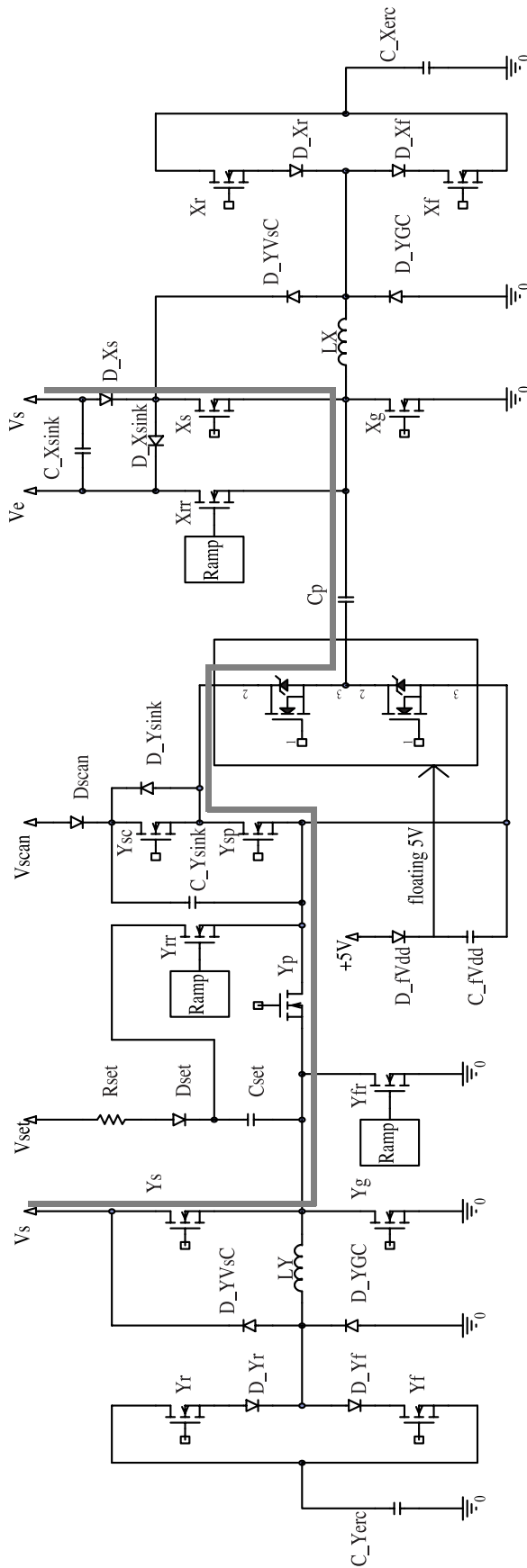
5-2-3(E) DRIVER BOARD CONNECTOR LAYOUT

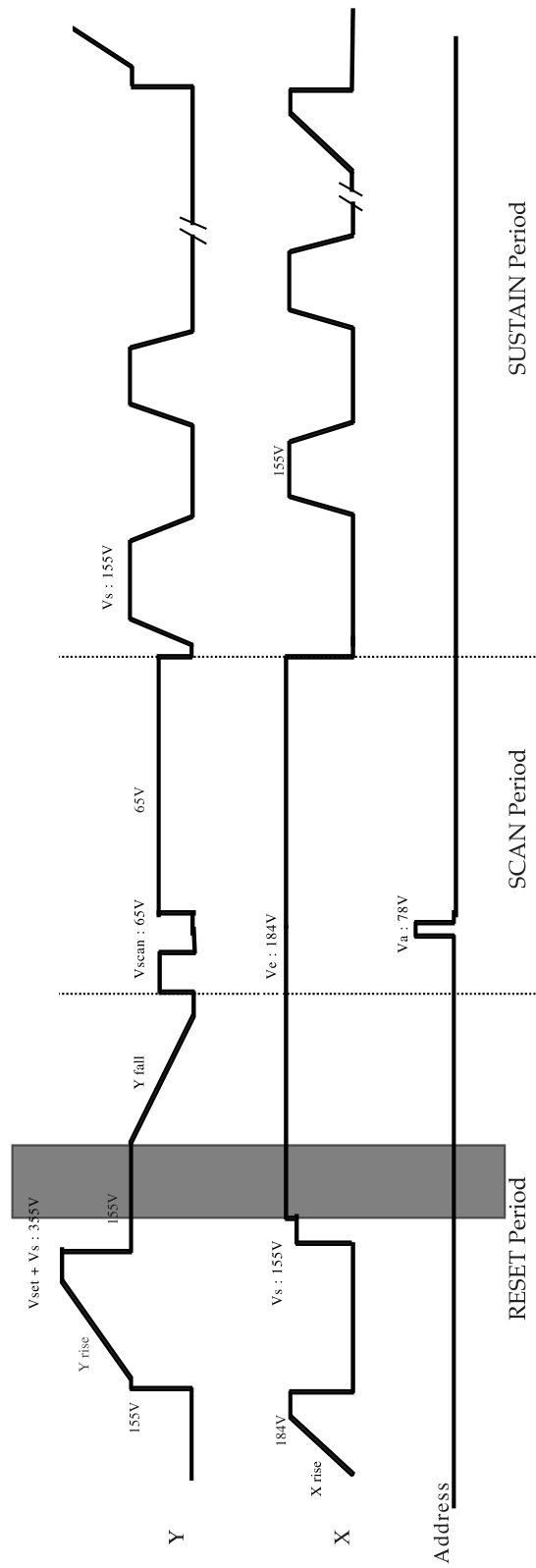
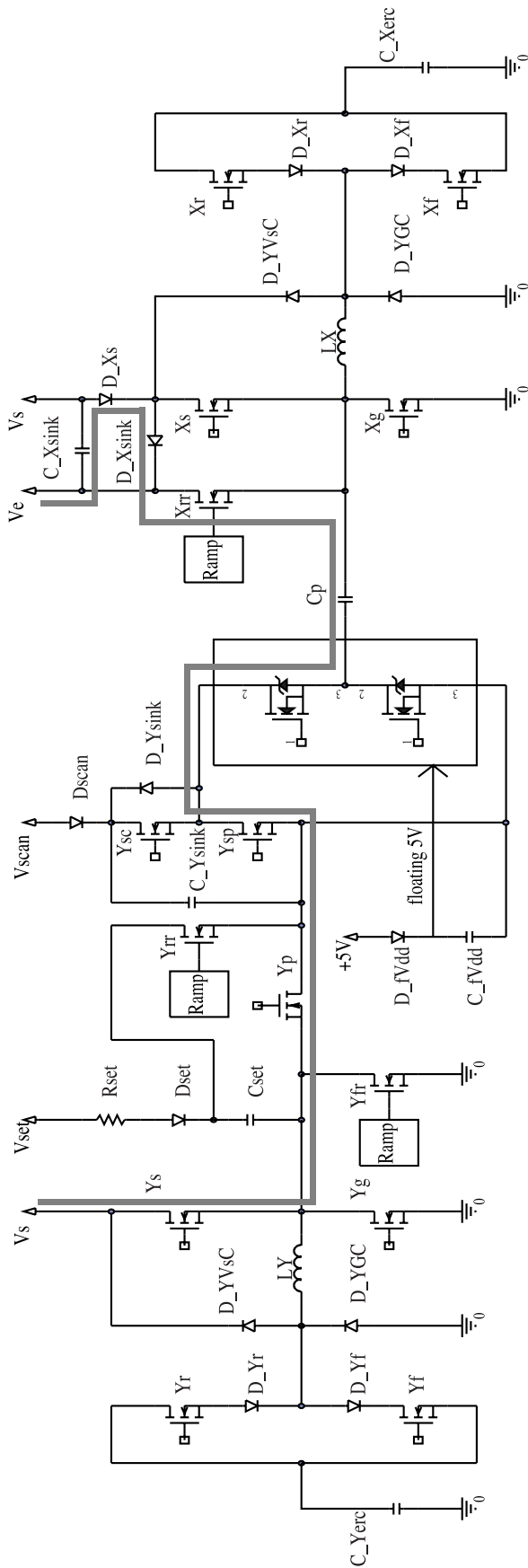


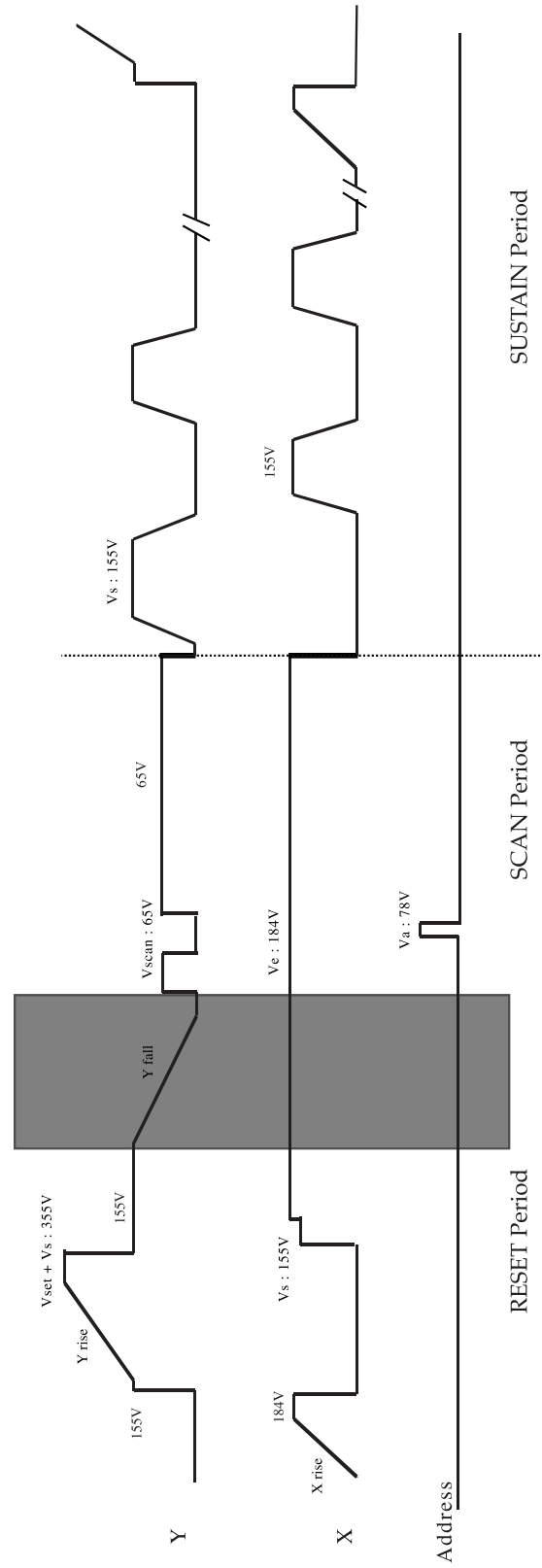
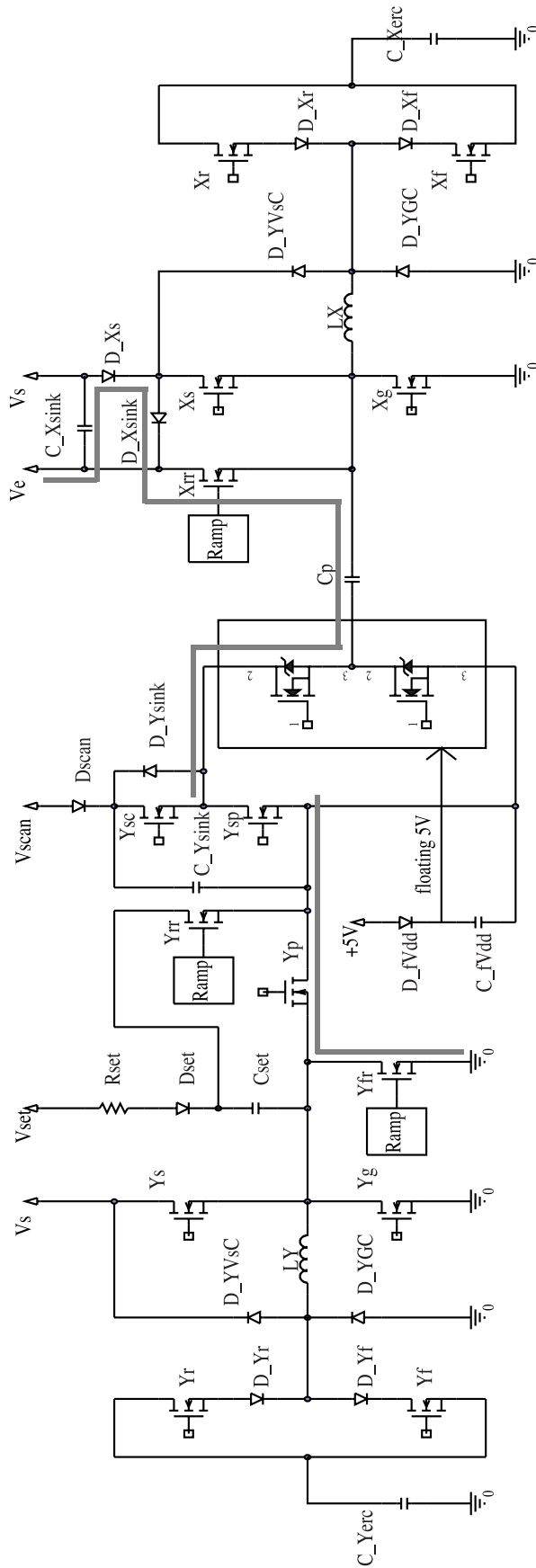


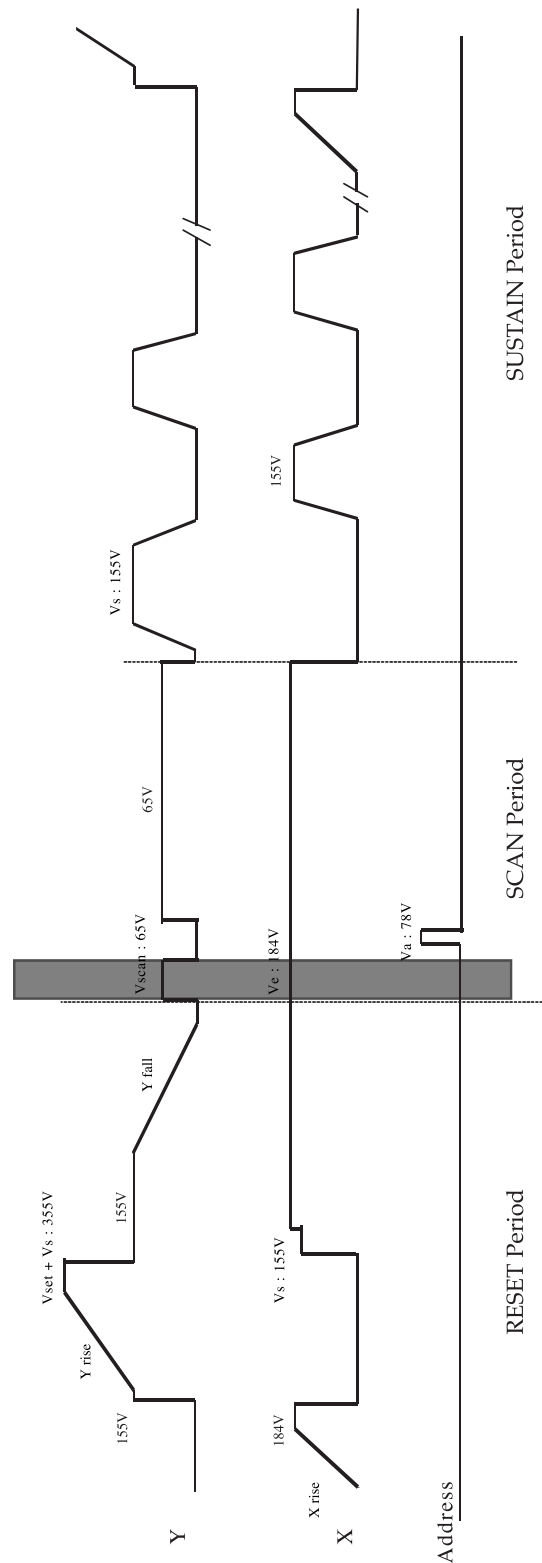
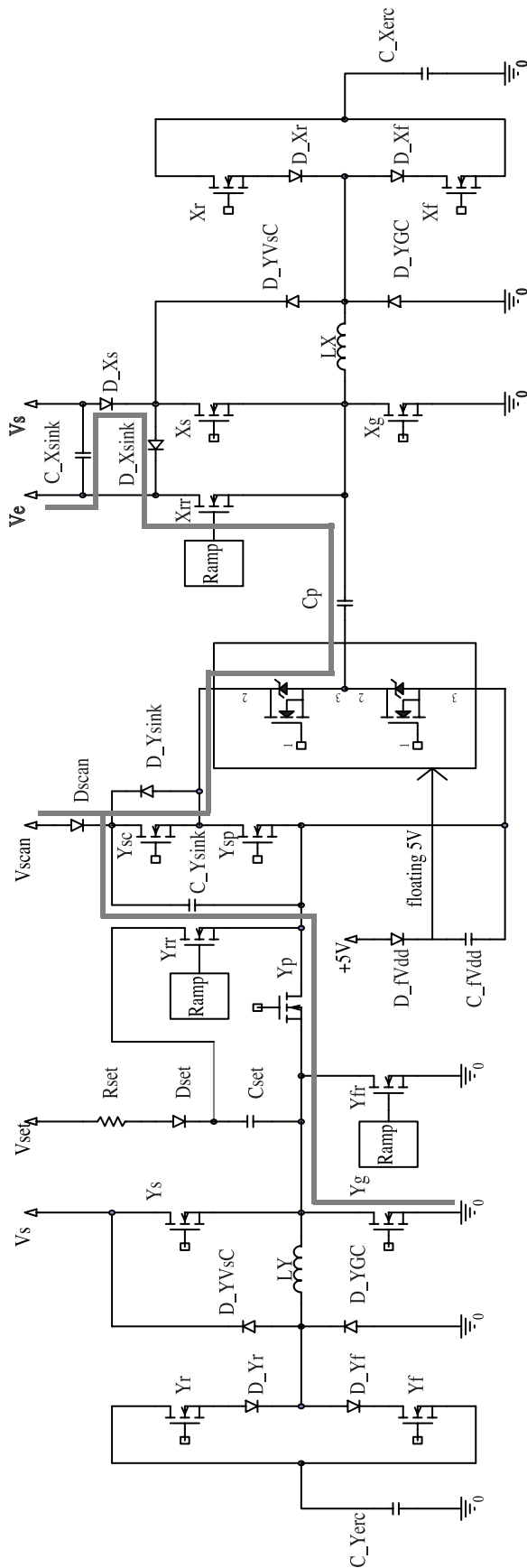


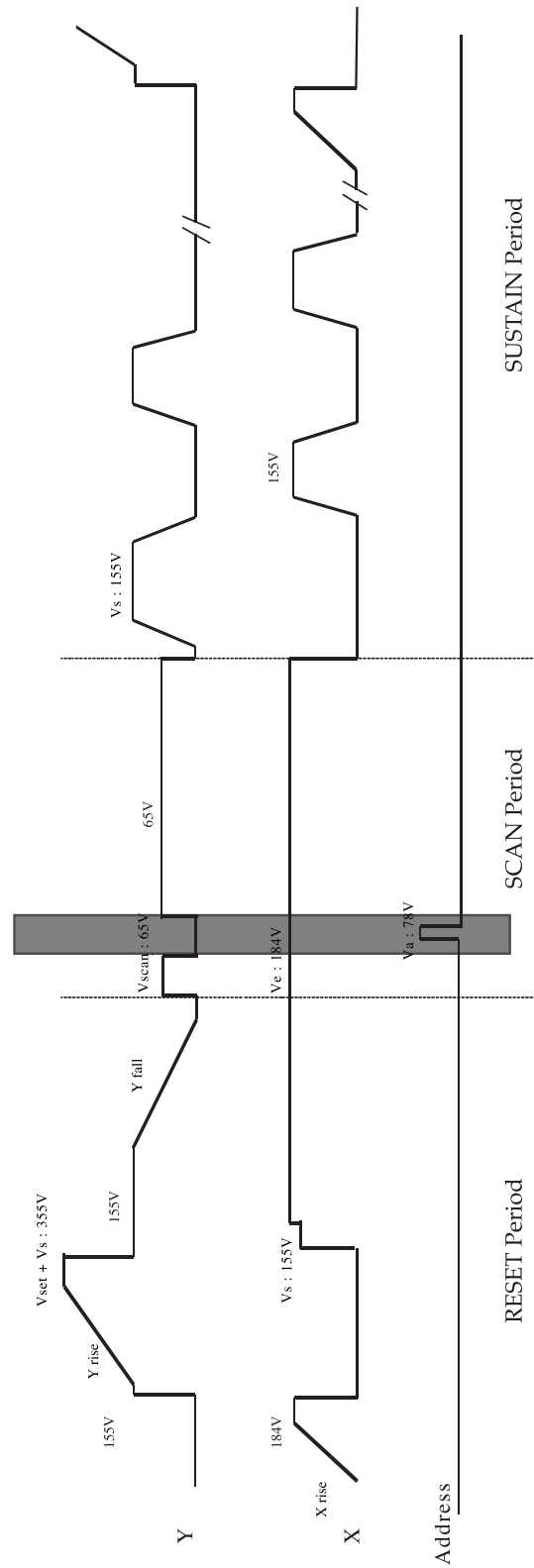
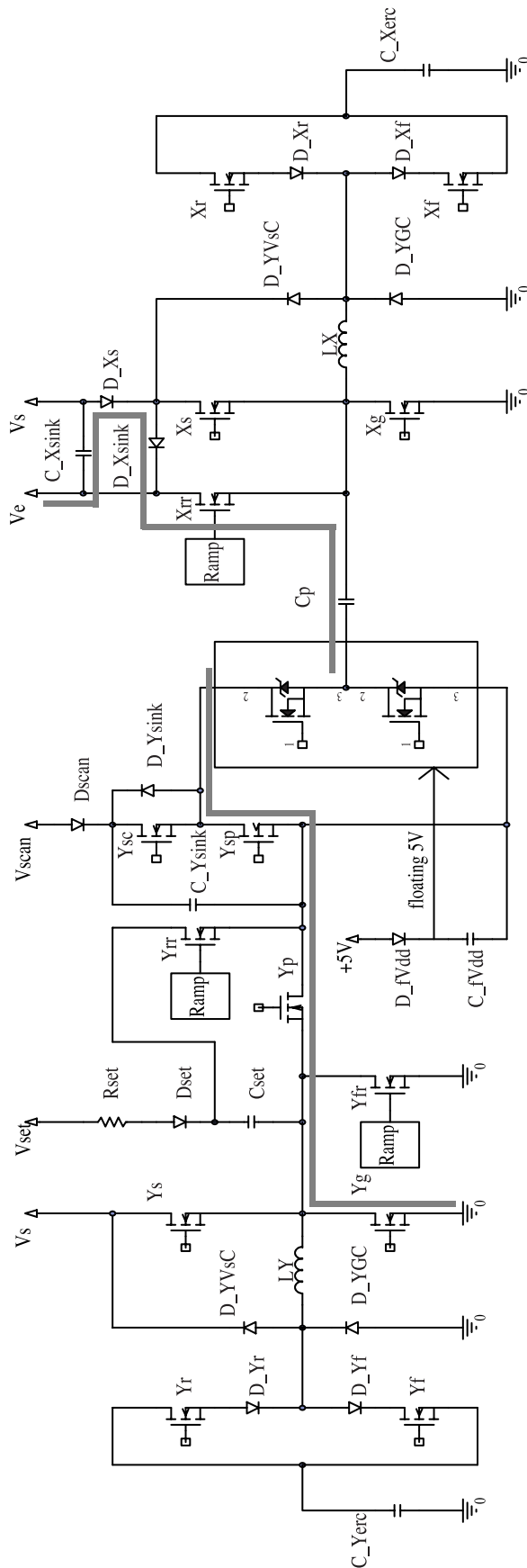


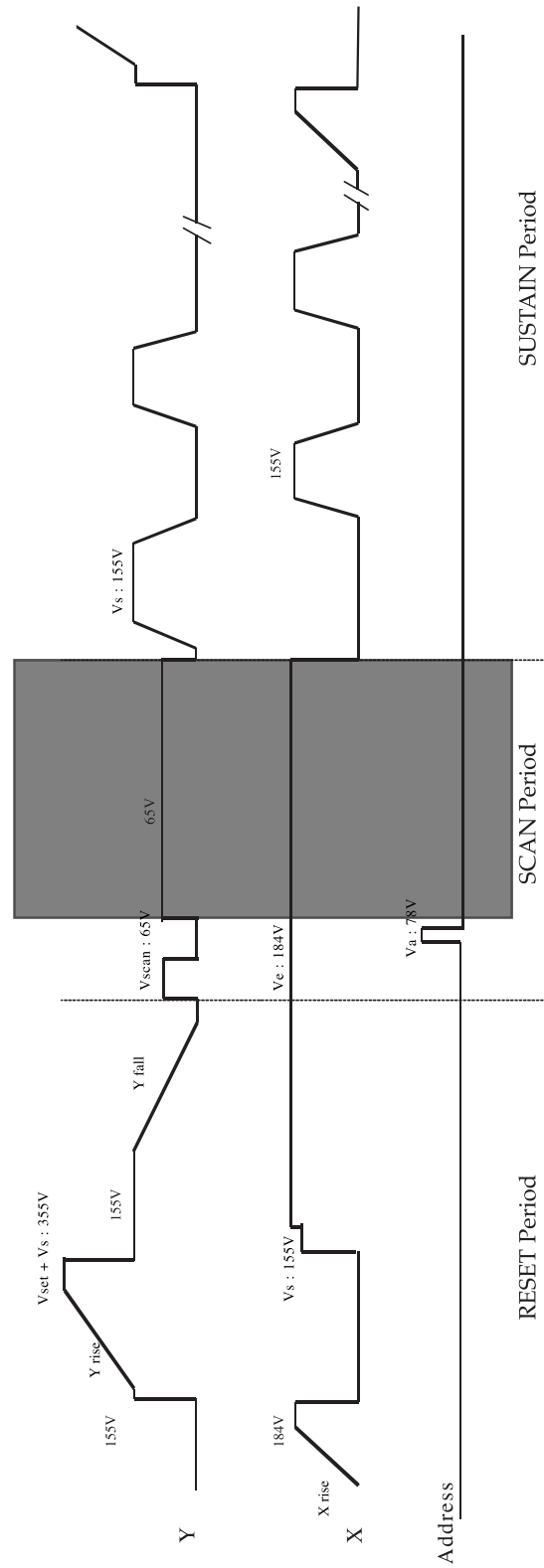
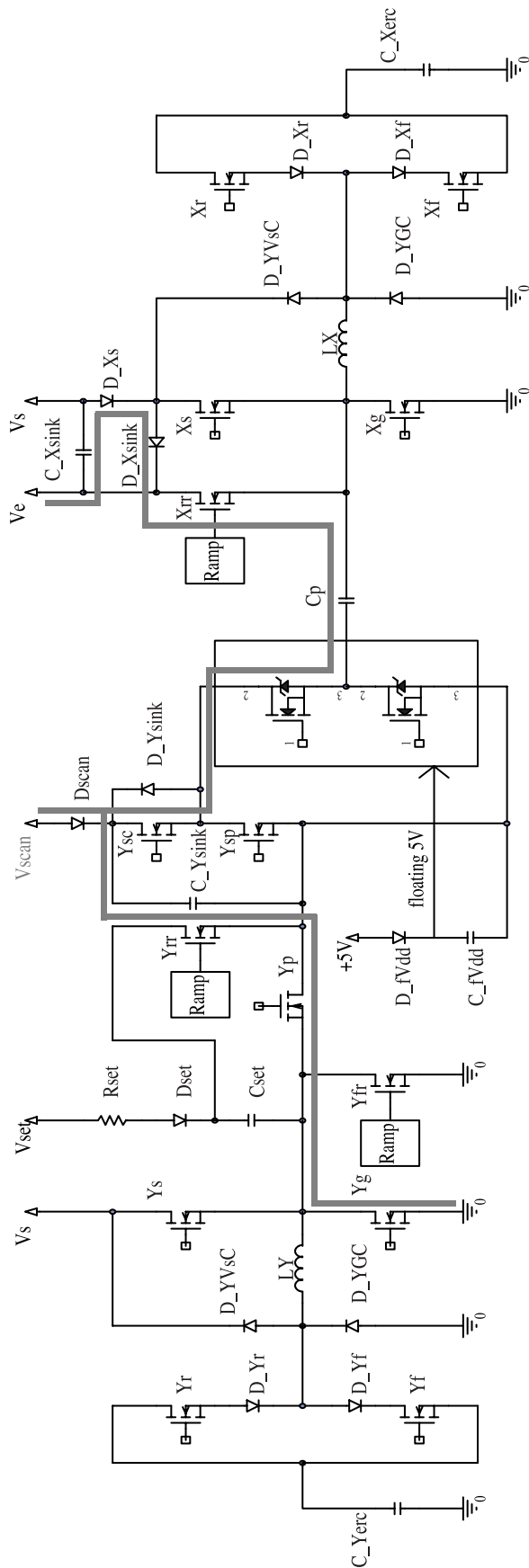


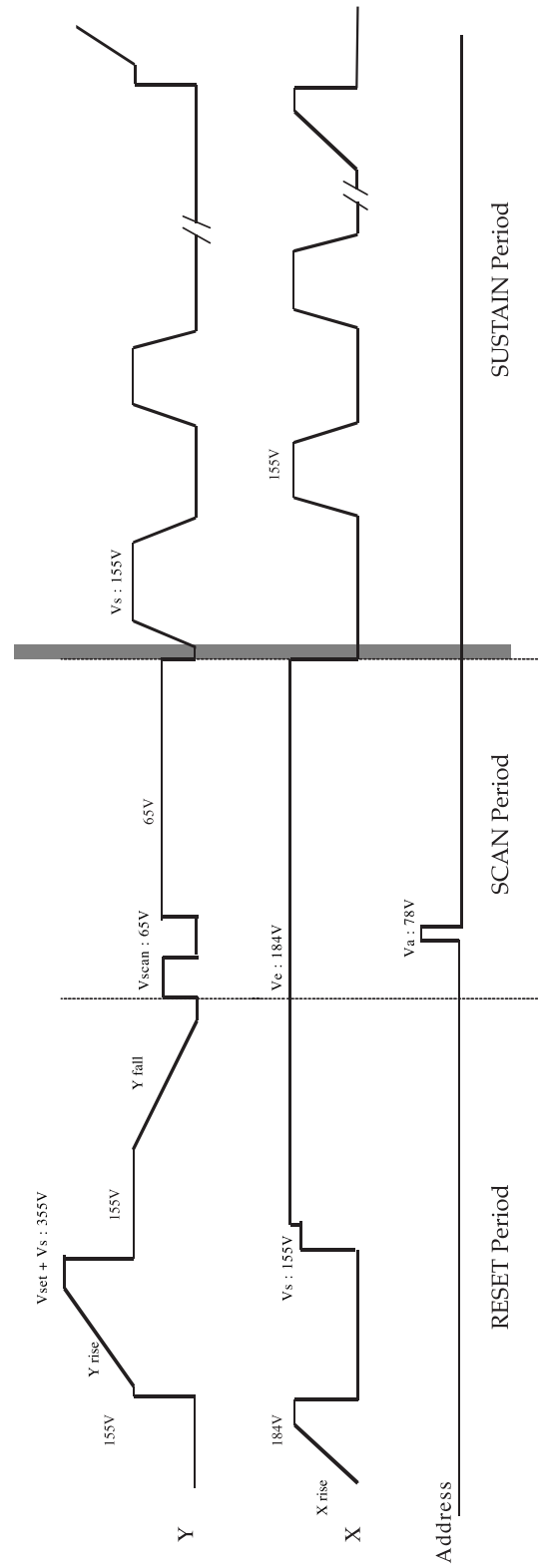
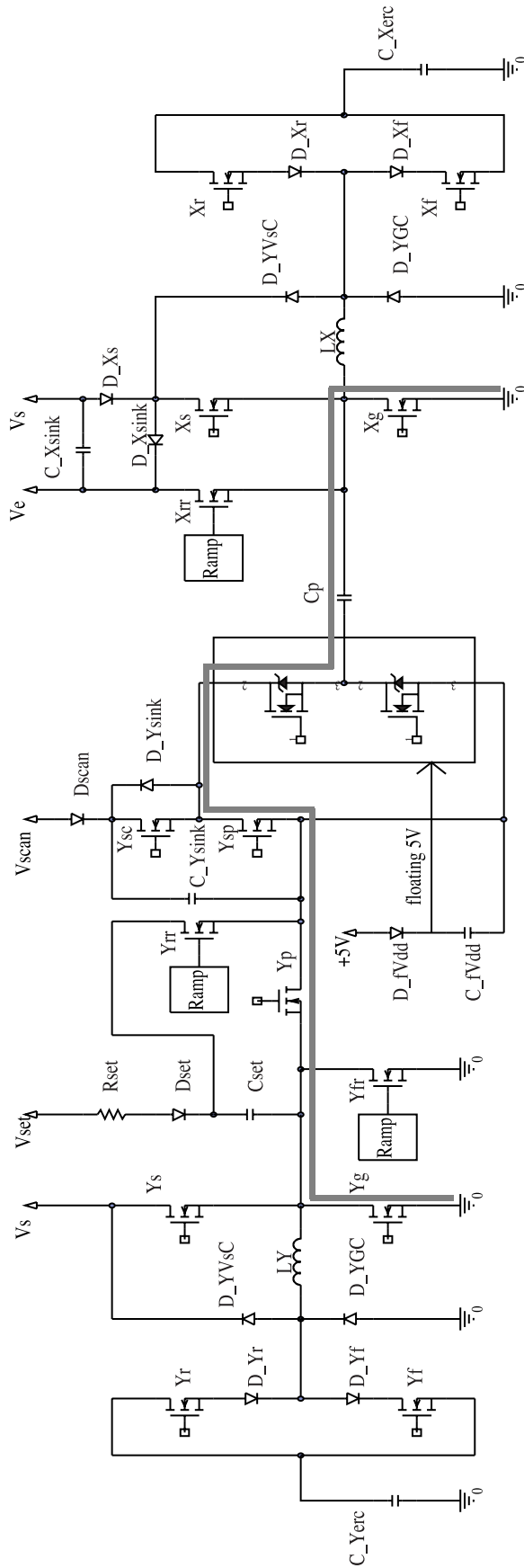


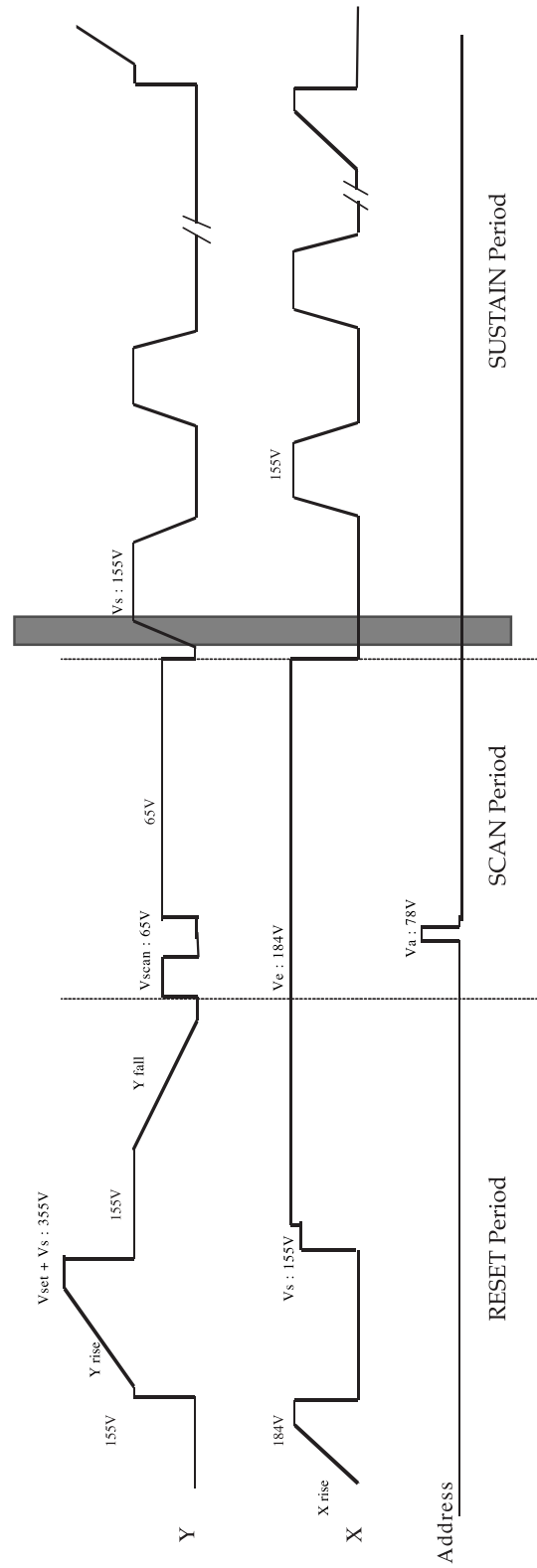
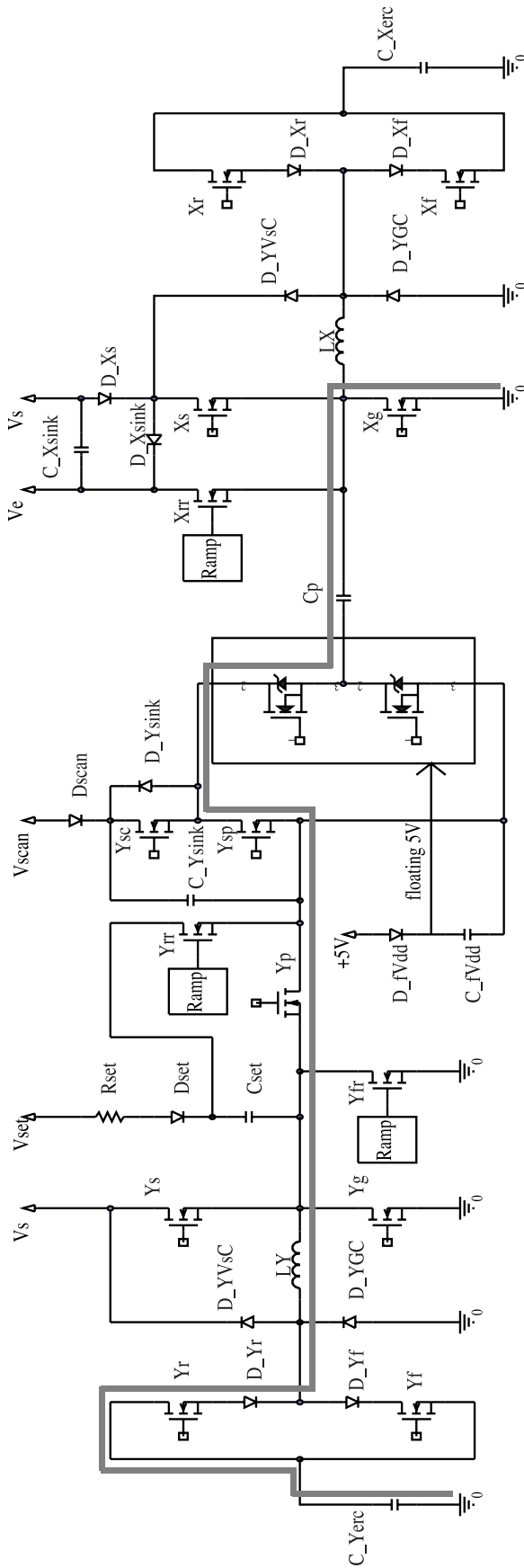


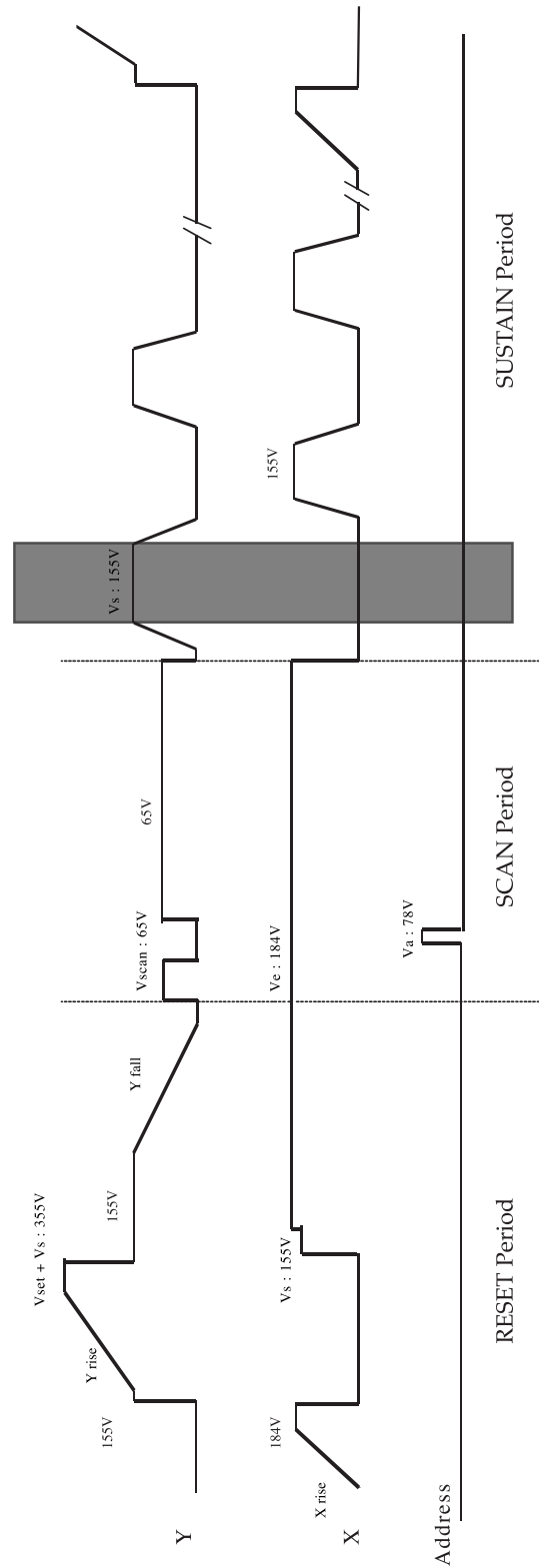
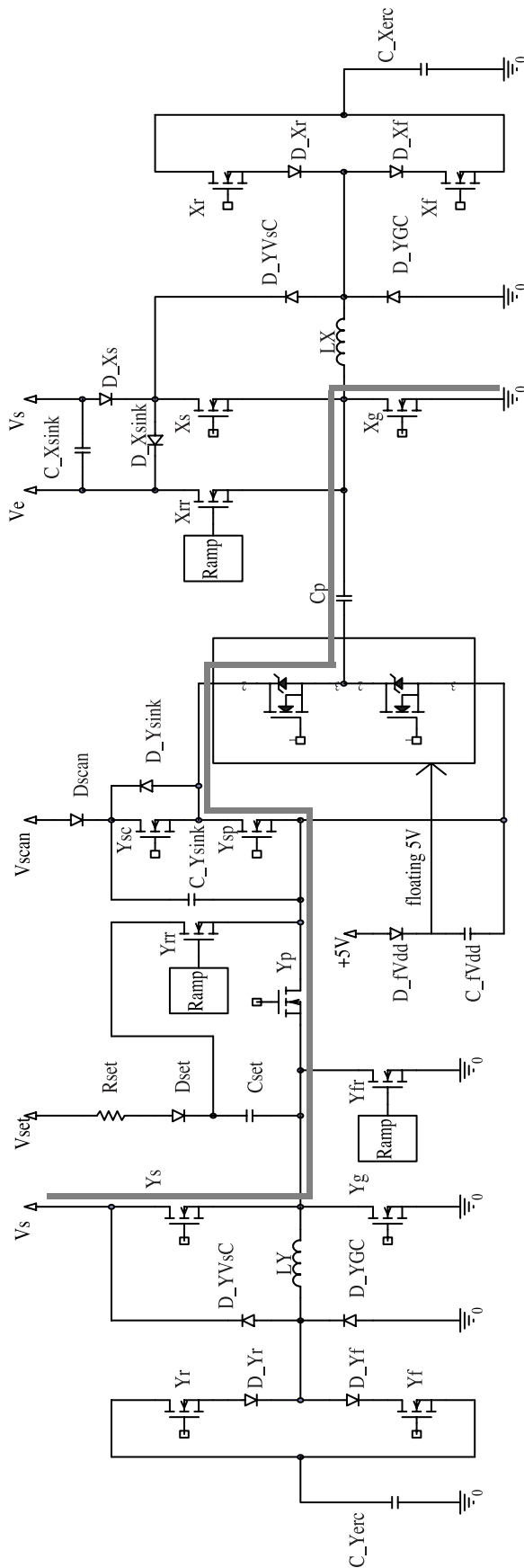


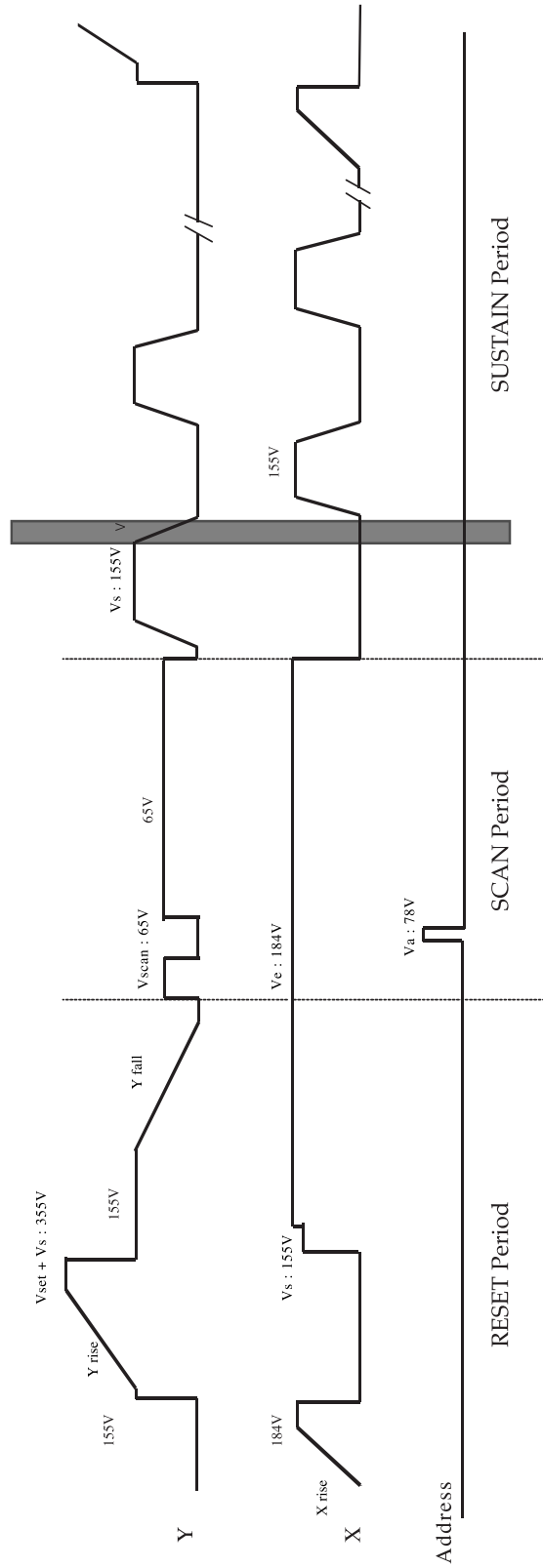
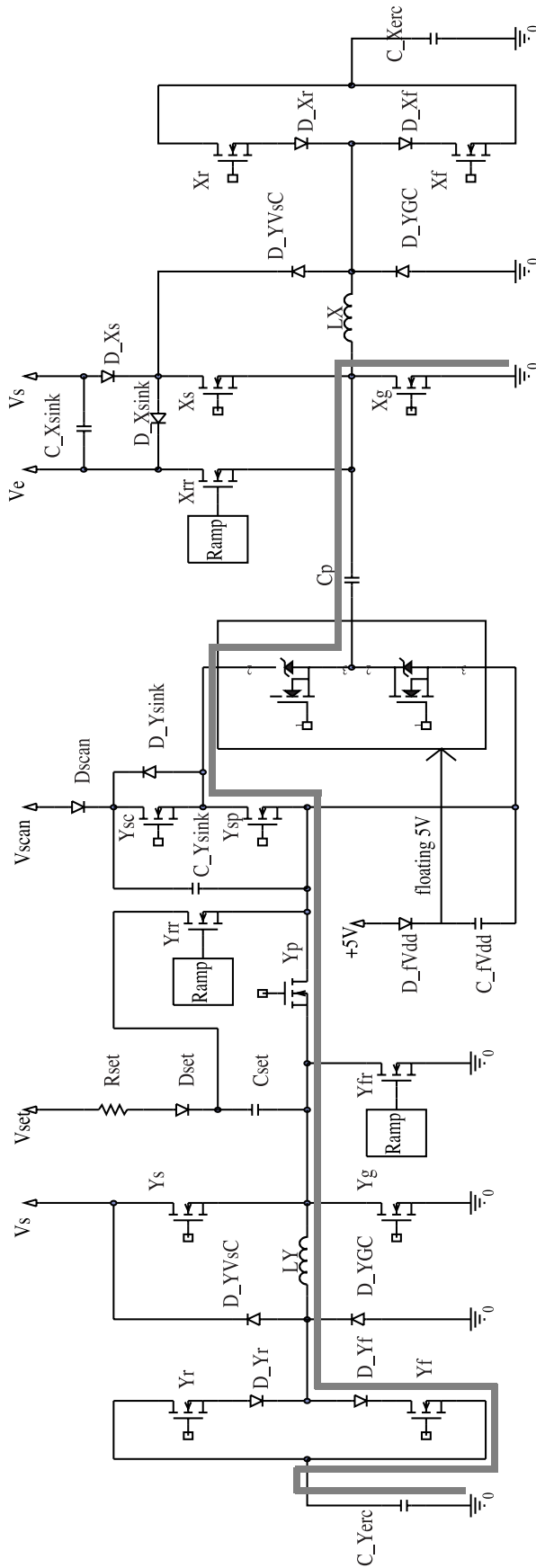






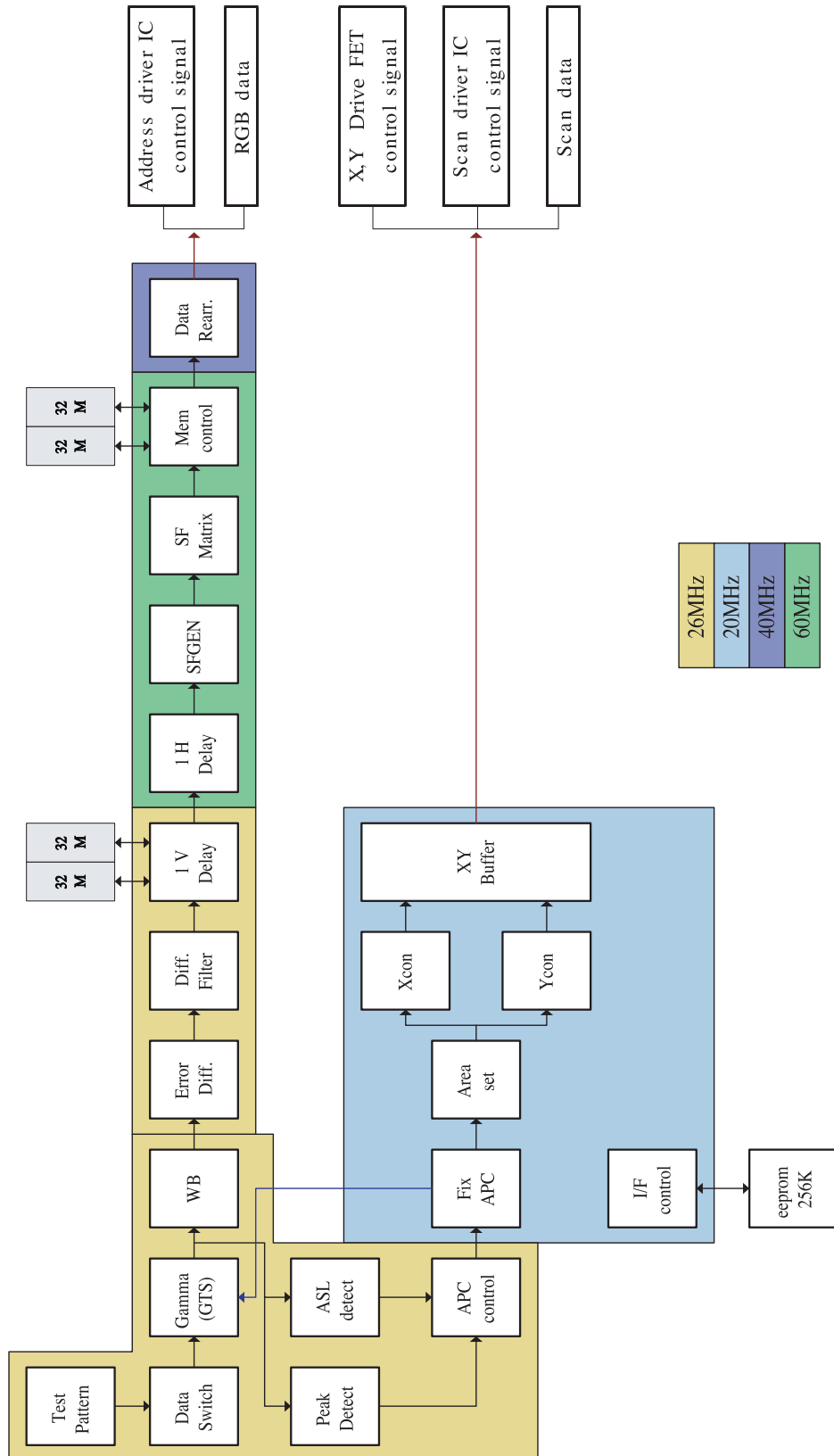






5-3 Logic part

5-3-1 Logic Board Block diagram

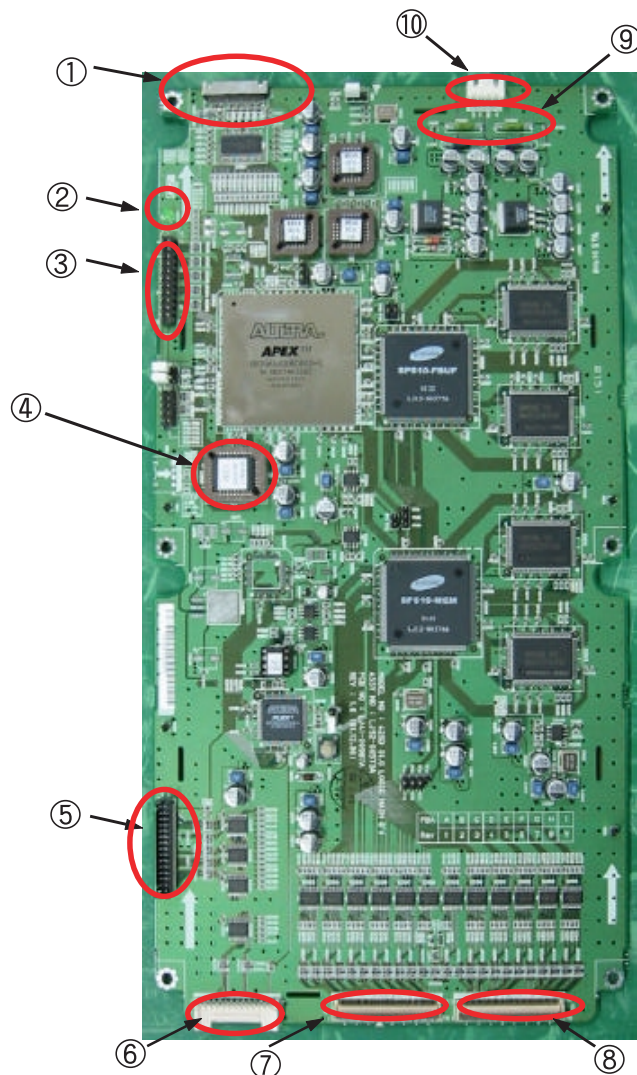


5-3-1(A) TDESCRIPTION OF LOGIC BOARD

The logic board consists of the logic main board and the buffer board. The logic main board processes video signal, and then generates and outputs address driver output signal as well as XY drive signal. The buffer board buffers address driver output signal, and sends it to the address driver IC (COF module).

Logic Board		Function
Login Main		<ul style="list-style-type: none"> - Processes Video signal (W/L, Error diffusion, APC). - Outputs address drive control signal and data signal to buffer board. - Outputs XY drive board control signal.
Buffer board	E Buffer board	Sends data signal and control signal to left-bottom COF.
	F Buffer board	Sends data signal and control signal to right-bottom COF.

5-3-1 (B) NAMES AND DESCRIPTION OF THE MAIN COMPONENTS OF THE LOGIC BOARD



NO	Name	Function
1	LVDS Connector	An input connector to receive LVDS encoded RGB, H, V, DATAEN, and DCLK signal from the video board.
2	Operation LED	Shows the logic board properly receives Sync and clock signal. (Normal: Blinks at 1 second interval)
3	Key-Scan Connector	A connector to connect key scan board checking and adjusting 24C16 data.
4	256k	An EEPROM to save gamma table, APC table, drive signal timing and other options.
5	Y Connector	A connector to output Y drive board control signal.
6	X Connector	A connector to output X drive board control signal.
7	LE01 (Address Buffer Connector)	A connector to output address data and control signal to the E, F buffer board.
8	LE02 (Address Buffer Connector)	A connector to output address data and control signal to the E, F buffer board.
9	Power Fuse	A fuse connected to the power source (5V) input to the logic board.
10	Power Connector	A connector to supply power (5V) with the logic board.

5-3-1(C) WAVEFORMS IN NORMAL OPERATION

If the PDP unit and the logic board are operating properly, the operation LED in the figure will blink at about 1 second interval.

If the set doesn't operate normally, first check the status of the operation LED through eye-inspection, and then replace the board. To check and troubleshoot, follow the logic board test procedures attached in appendix.

4 Troubleshooting for 42" SD s1.0 logic main board

Required test equipment : - Oscilloscope (digital 400 MHz 3 channel or more)
 - Multi meter

Other equipment : - DC power supply (5V: 1EA)
 - Sub-PCB ASS'Y for JIG: 1 EA

- ① First, perform eye-inspection and short circuit inspection on the power stage of the logic board to examine. If no problem is found, perform the following examinations on the board in order.
- ② Replace IC2017(256K EEPROM) of the logic board with Test EERPOM. Change the clock setting of the logic board to internal. (Refer to the setting procedures described on the next page.)
 - fl If there is no available Test EEPROM, you can use PG 00 for Windows NT systems, or PG 40 for NT/PAL compatible systems by setting address 20 to 81, 22 to 00, 23 to 00, and 70 to 01.
- ③ Connect power(5V) to LD1, and check that LED(LD2000) on the left top of the board blinks at about 1 second interval.
- ④ If the logic board doesn't operate normally, the LED will blink too fast or not be lighted on.
- ⑤ If no problem is found in the above examination, connect sub-PCB for logic output check, measure output waveform, and then compare the waveform with the appended waveform in normal operation. Record either OK or NG after examination.
- ⑥ Check the drive Y s/w, the drive X s/w, and the address signal in order.
- ⑦ Set probe 1 of oscilloscope to trigger signal and connect it to the TP31 of the logic board.
- ⑧ Set the oscilloscope to 2ms/div. After adjusting probe 2 to 5V/div, check the output signal.
- ⑨ After troubleshooting is complete, turn off the power supply and disconnect connector.

1) Layout and Appearance of the board
(1) Layout of the logic main board

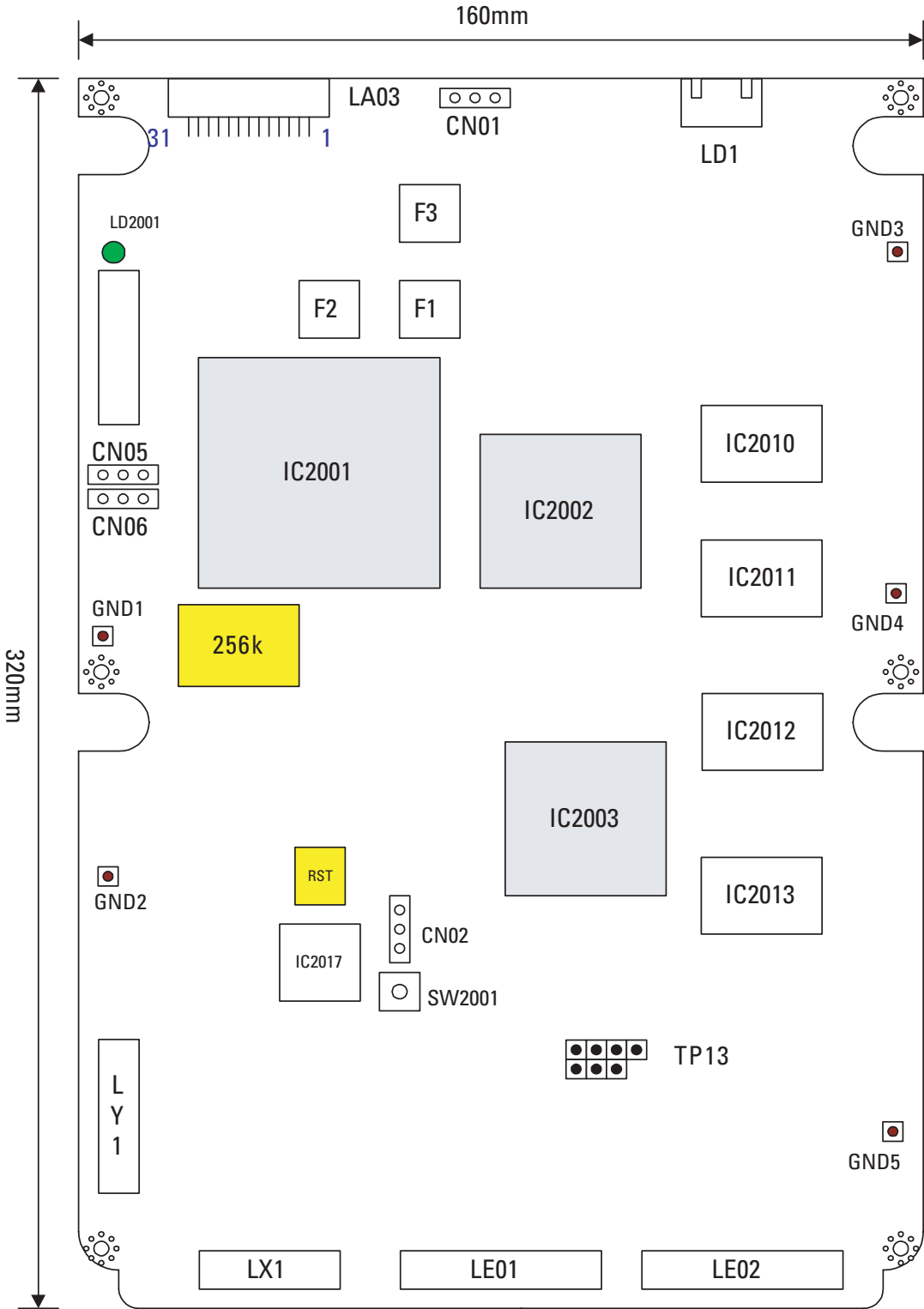


Figure 1. Layout of the logic main board

(2) Appearance and indication of connector
Basically, it is depicted on the PCB exactly same as the real one.

2) Jumper setting to select internal clock or external clock (CN01)

On the top of the logic main board, there is an option jumper, CN01 that allows switching between internal and external clocks. (Refer to Figure 1.) While troubleshooting, set it to internal clock as Figure 2 shows.

- 1. The jumper will be stocked set to external clock. Set it to internal clock during troubleshooting, and reset to external clock after examination.

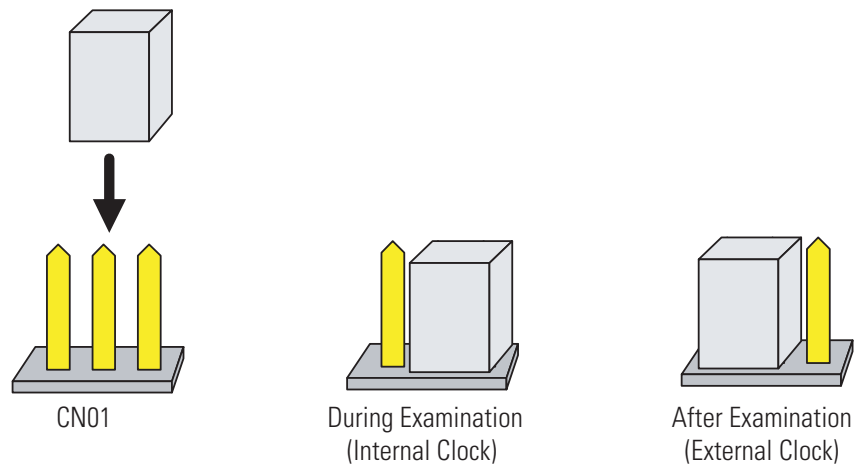


Figure 2. Jumper setting to select internal clock or external clock

3) Reset jumper setting (CN02)

The CN02 connector of the logic main board should be set to Reset signal as the following figure shows. It is default setting and should not be changed.

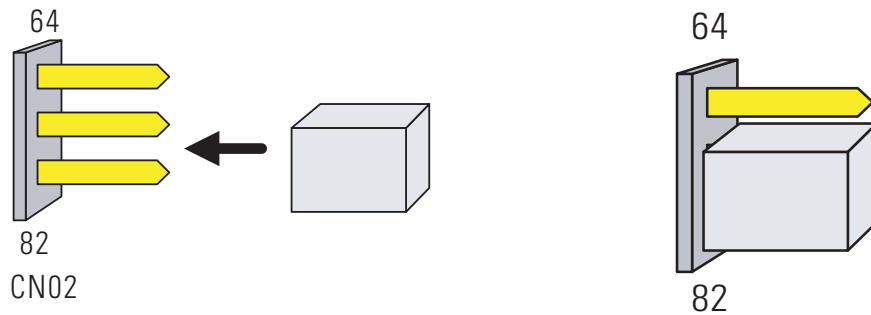


Figure 3. RESET JUMPER SETTING

- 4) Setting to select Internal pattern or external pattern (CN05)
 Default setting is external pattern.

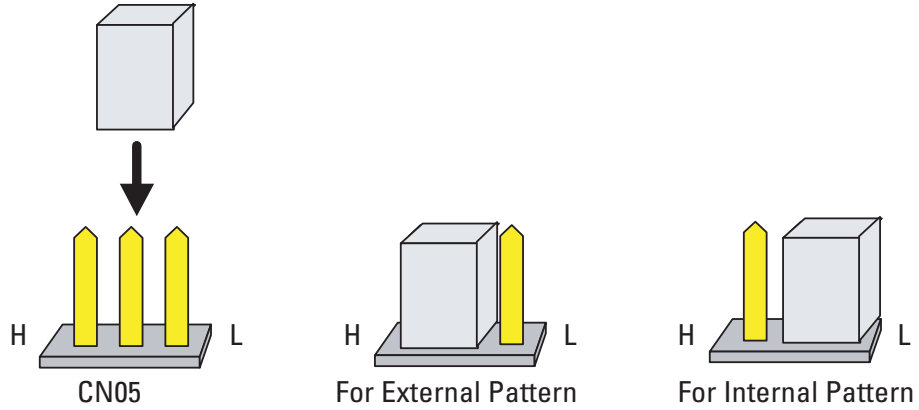


Figure 4. Jumper setting to select internal or external pattern

- 5) Jumper setting to select NTSC or PAL when internal pattern is selected (CN06)
 Switching between NTSC and PAL as following figure shows only works in internal pattern setting.
 Default setting is PAL mode.

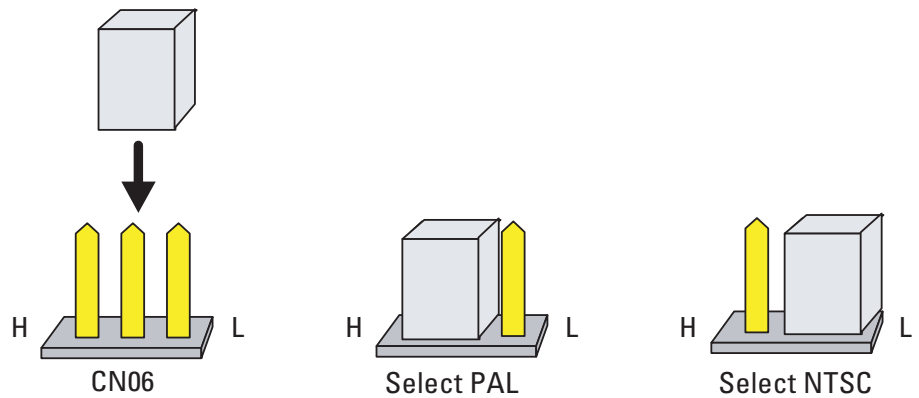


Figure 4. Jumper setting to select internal or external pattern

6) Using ASSY examination system

(1) Setting

- ① Preadjust the output voltage to 5V when using the linear power supply.
Also, check if the output voltage is 5V when using SMPS.
- ② Install the TEST PROM 256K, RST, F1, F2, and F3 on the logic main board.
To prevent misinsertion, make sure that the pin 1 of the PROM is inserted in the proper location marked on the PCB.
- ③ As shown in Figure 6, connect the logic main board and the JIG board for examination using the cables connecting LX1(13P), LY1(30P), LE01, and LE02(80P).
- ④ Set the oscilloscope to 5ms/div, 2V/div.
Connect the probe 1 as Figure 7 shows and set it to a trigger.

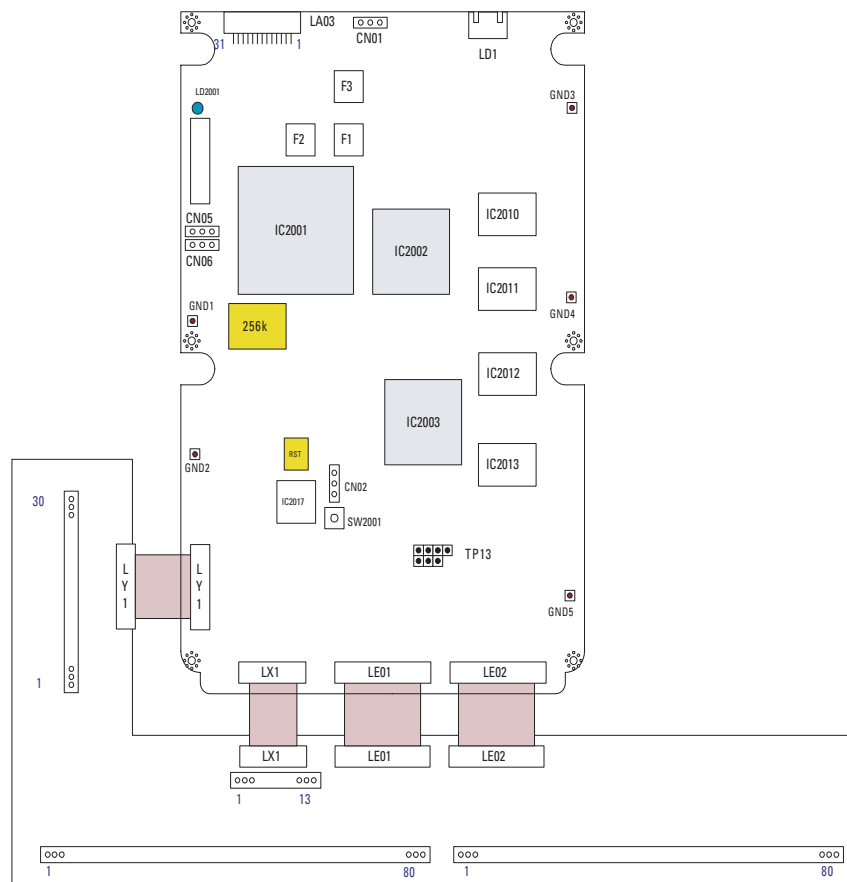


Figure 6. Connecting between the logic main board and the JIG board for examination

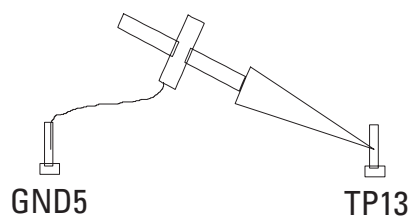


Figure 7. Connecting probe 1 of the oscilloscope

(2) Logic main board

① Set the logic main board as Figure 6 shows.

fl Check for the test PROM installation status and clock jumper setting.

② Connect a 4-pin connector cable between LD01 of the logic main board and the linear power supply (or SMPS).

fl Connect while the linear power supply (or SMPS) is turned off.

③ Turn the linear power supply on and supply 5V power to the logic main board.

Check if LED, LD2000 on the left top of the board blinks at about 1 second interval. If the logic board doesn't operate normally, the LED will blink too fast or not be lighted on.

④ Measure the waveform of each test point on the board, and then compare them with the appended waveforms.

You should examine the waveforms of all test points.

If the waveform of a test point is different from the appended waveform, or the voltage level is low, do not proceed to the next examination step and check other abnormal test points.

⑤ Perform RESET examination.

Press and hold SW2001 reset switch for 5 seconds to turn the LE2000 of the logic main board off. Release the switch after 5 seconds and check that LD2000 blinks. If no problem is found, finish the examination.

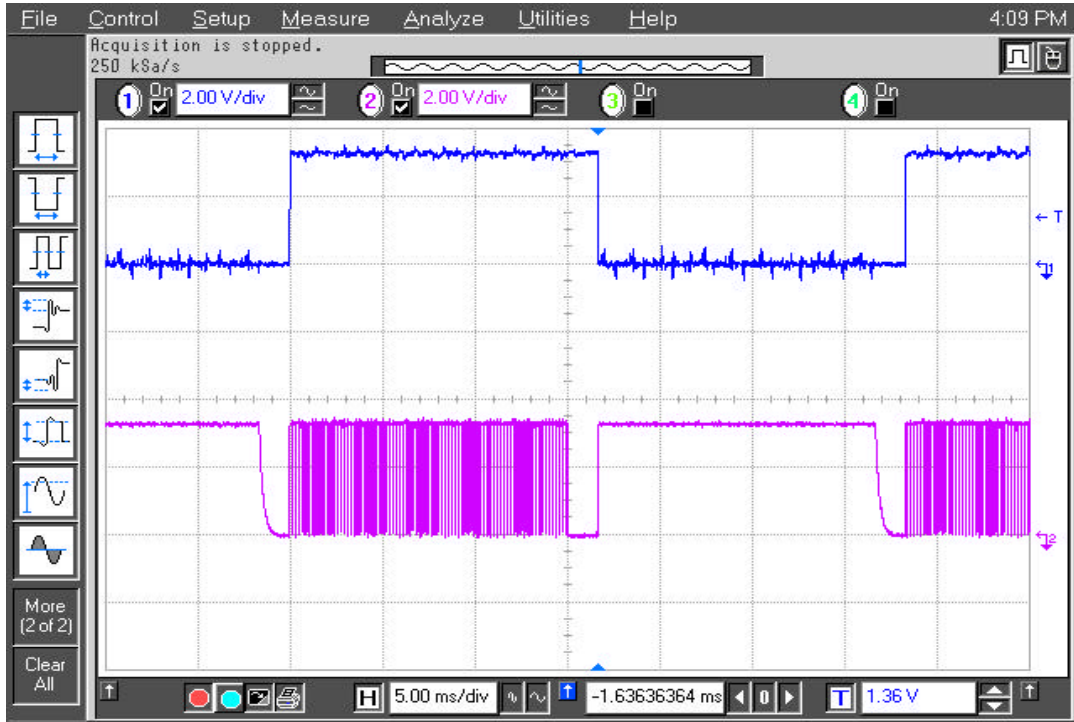
⑥ If the waveforms of all test points are output properly and RESET examination is complete, turn off the linear power supply (or SMPS) to finish examination.

⑦ After all examinations are complete, perform as follows.

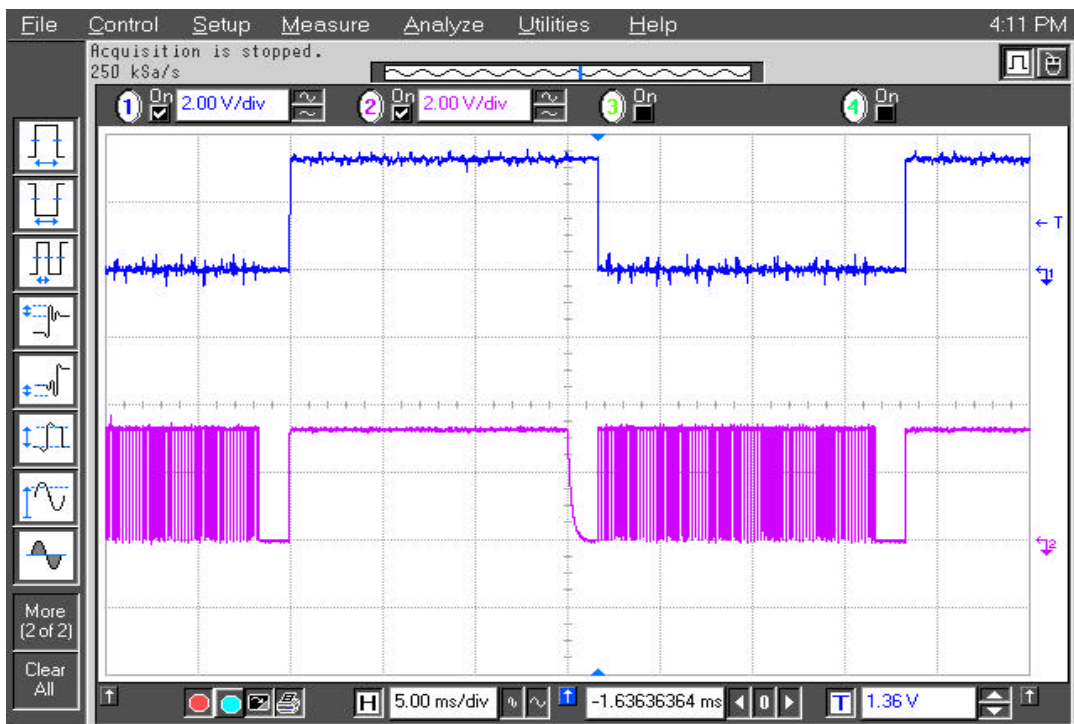
- Reset the clock jumper to external clock.
- Reset the internal/external pattern jumper to external pattern.
- Reset the NTSC/PAL mode jumper to PAL mode.

Board Waveform Test

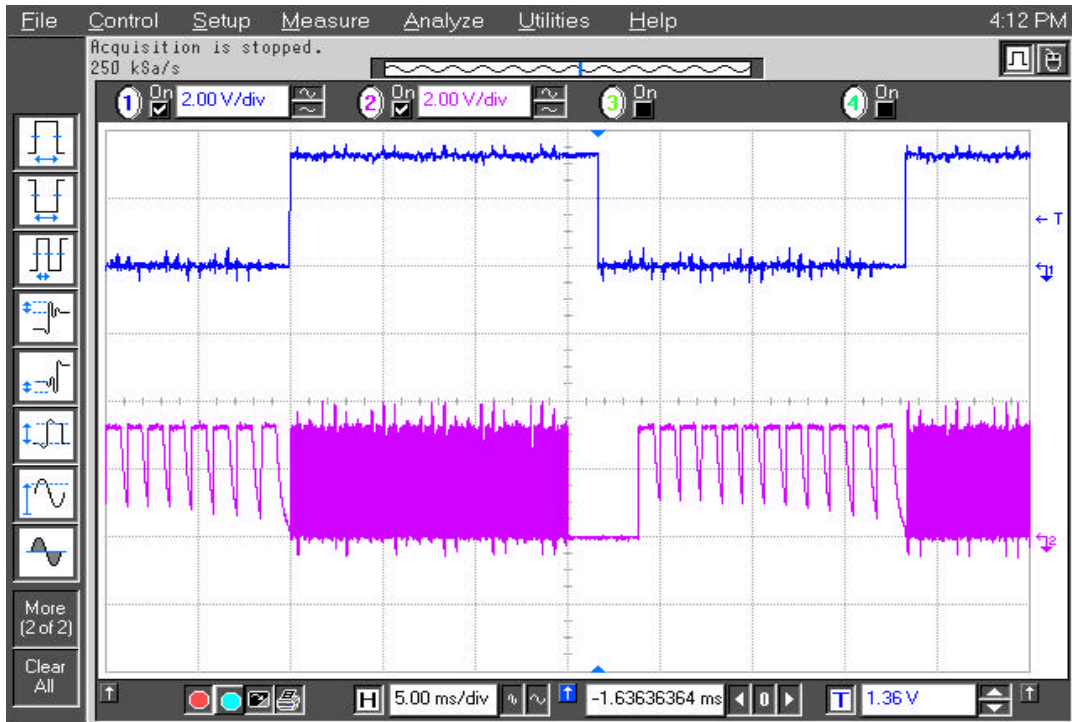
1. Check the waveform after pointing Probe2 at IC2005 pins 1, 72.



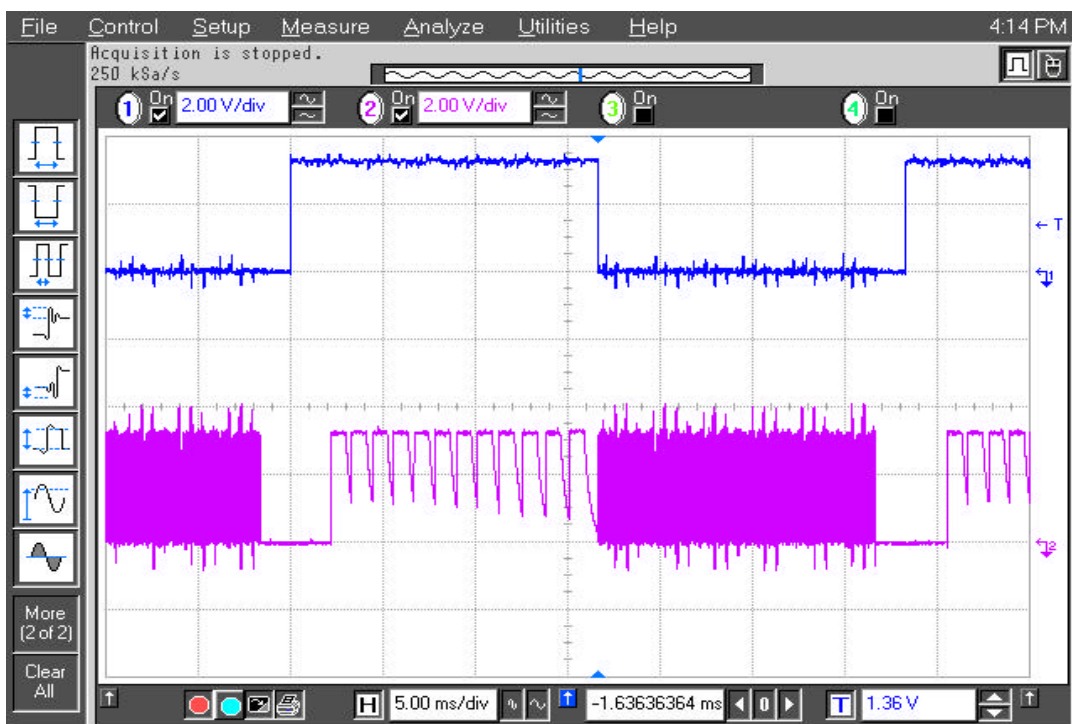
2. Check the waveform after pointing Probe2 at IC2006 pins 1, 72.



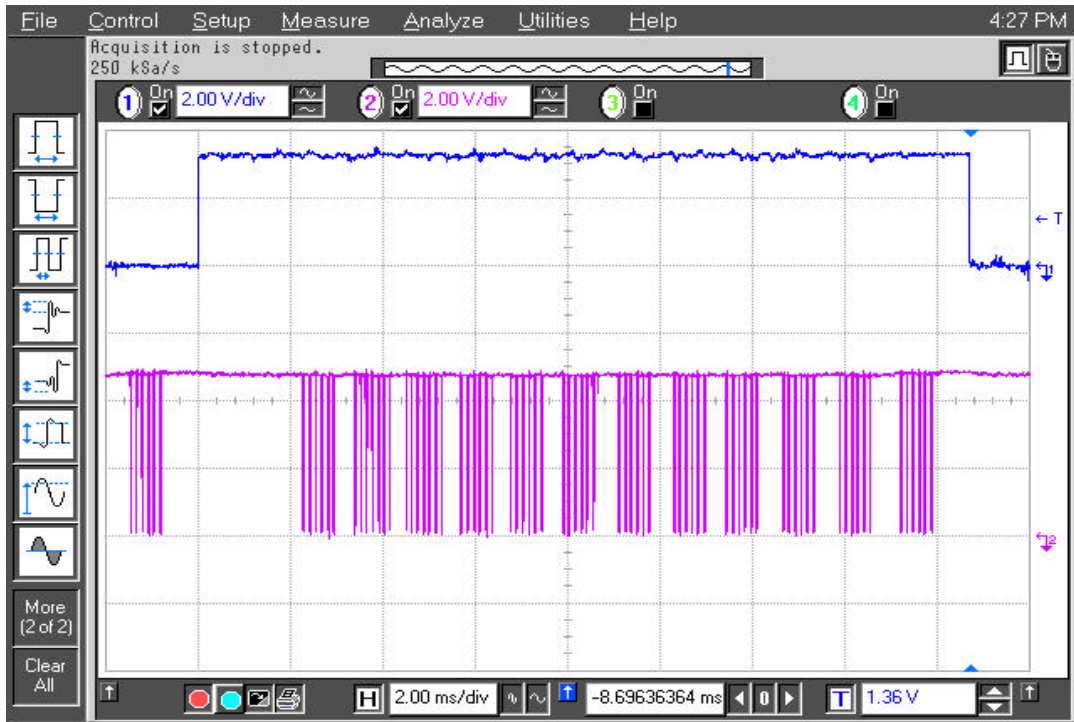
3. Check the waveform after pointing Probe2 at IC2007 pins 1, 81.



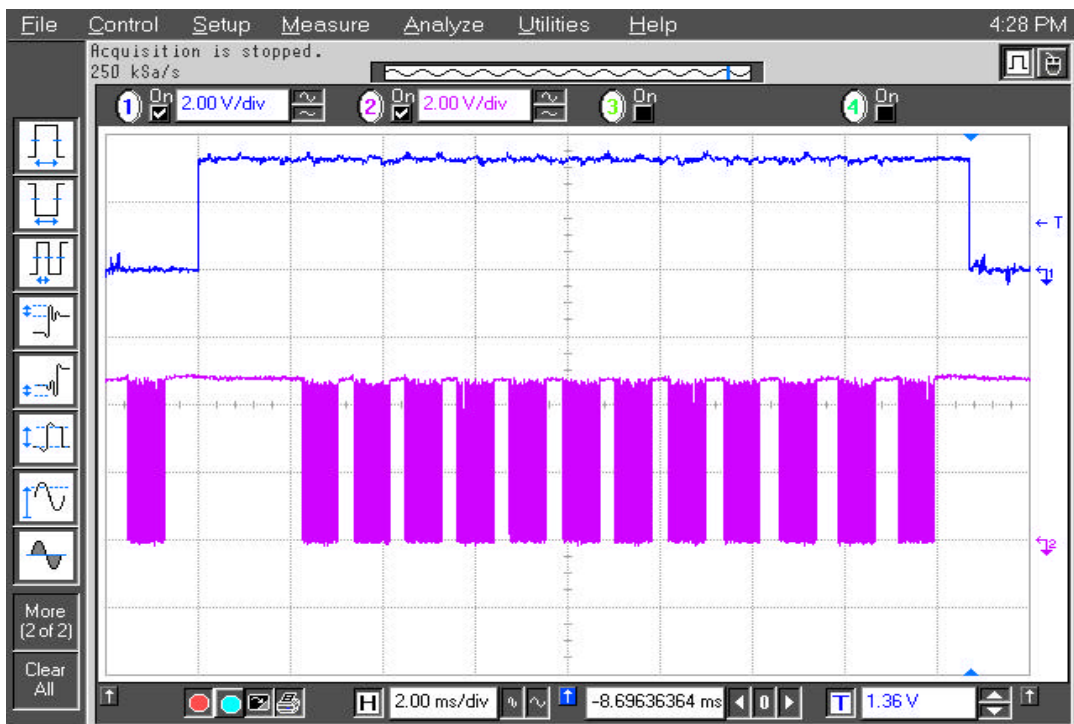
4. Check the waveform after pointing Probe2 at IC2008 pins 1, 81.



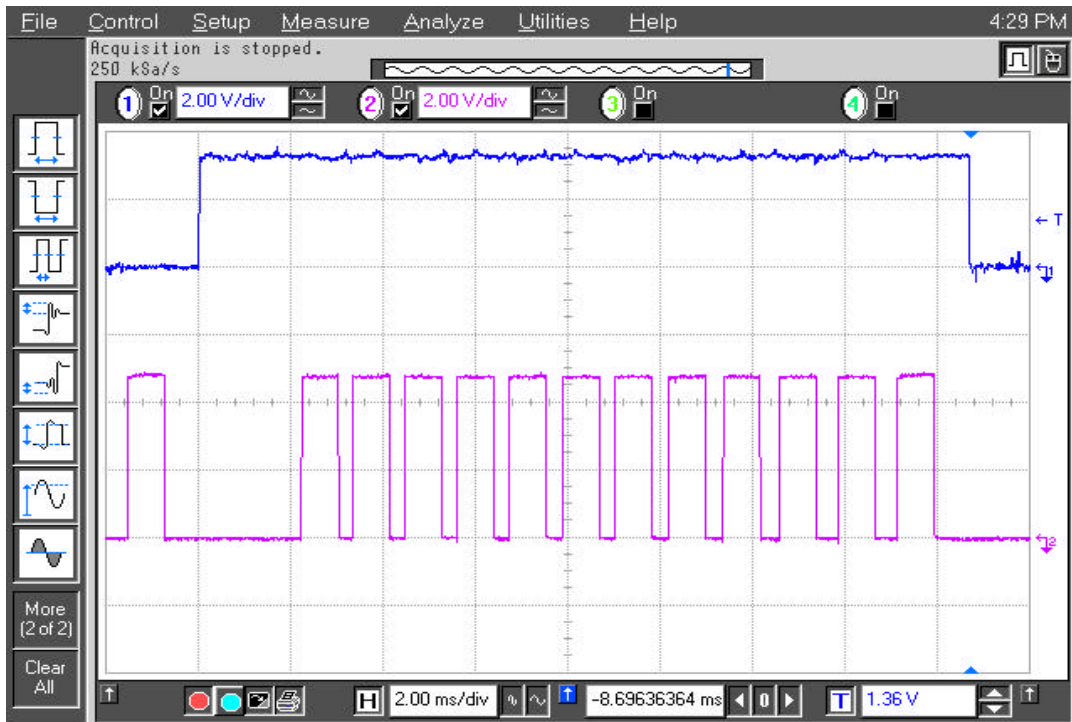
5. Point Probe2 at LY1 pin30 (F2016 pin8 (LE-Y) on the logic main board) on the jig board. (F2016: Array resistor)



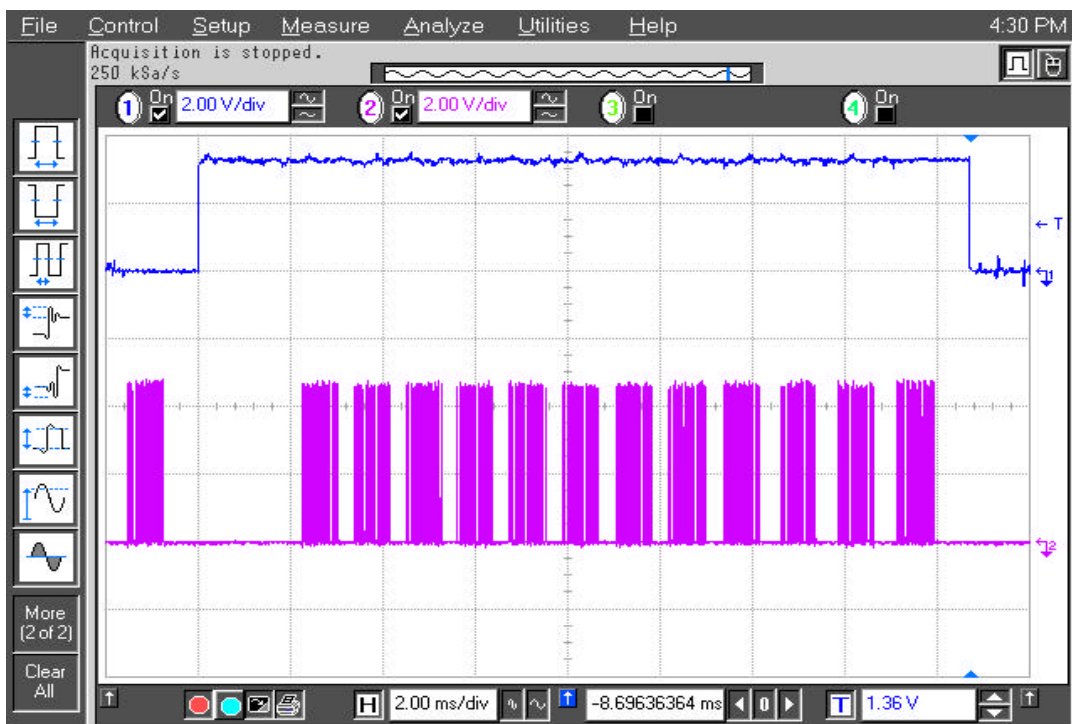
6. Point Probe2 at LY1 pin28 (F2016 pin7 (STB-Y) on the logic main board) on the jig board.



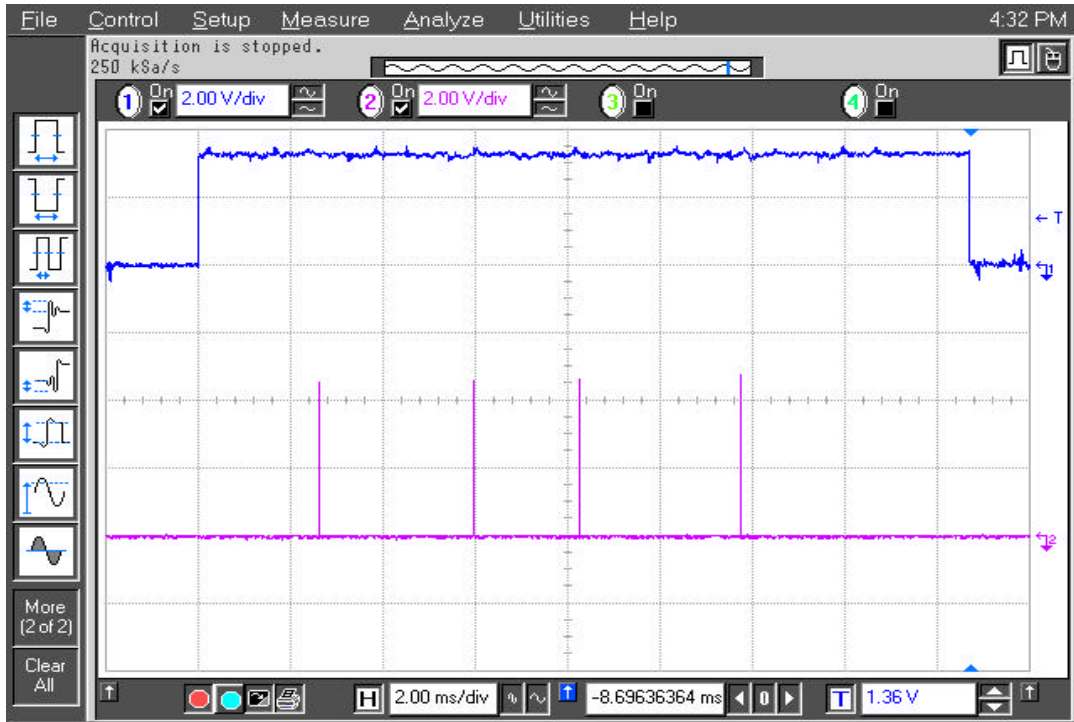
7. Point Probe2 at LY1 pin25 (F2016 pin6 (TCS-Y) on the logic main board) on the jig board.



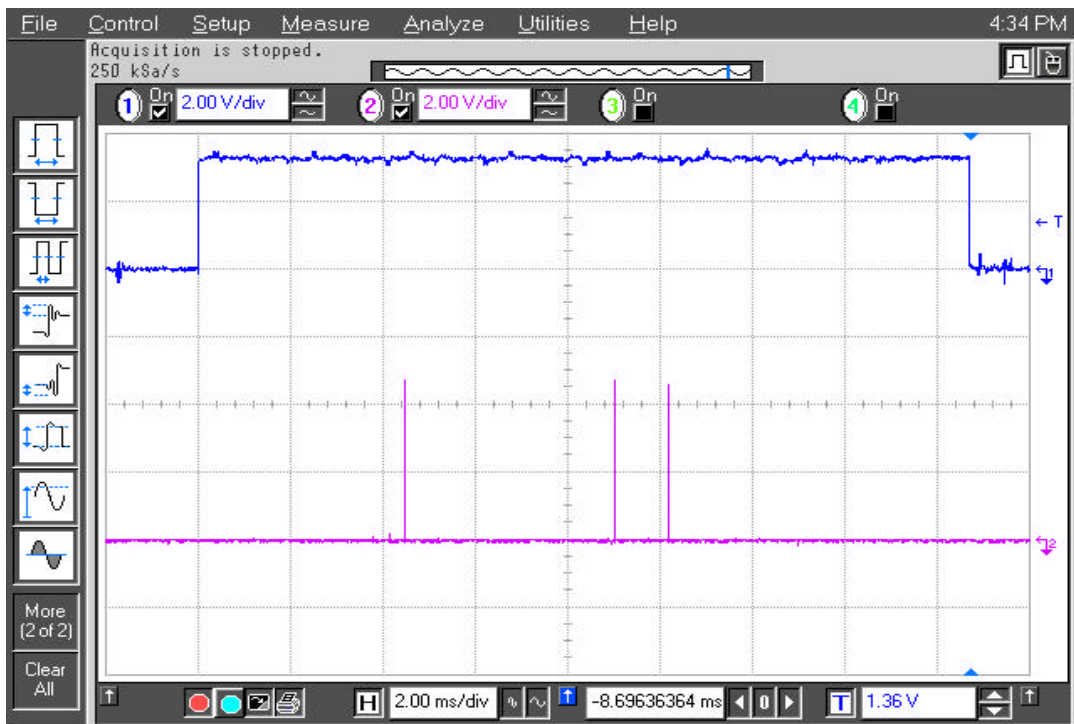
8. Point Probe2 at LY1 pin24 (F2016 pin5 (CLK-Y) on the logic main board) on the jig board.



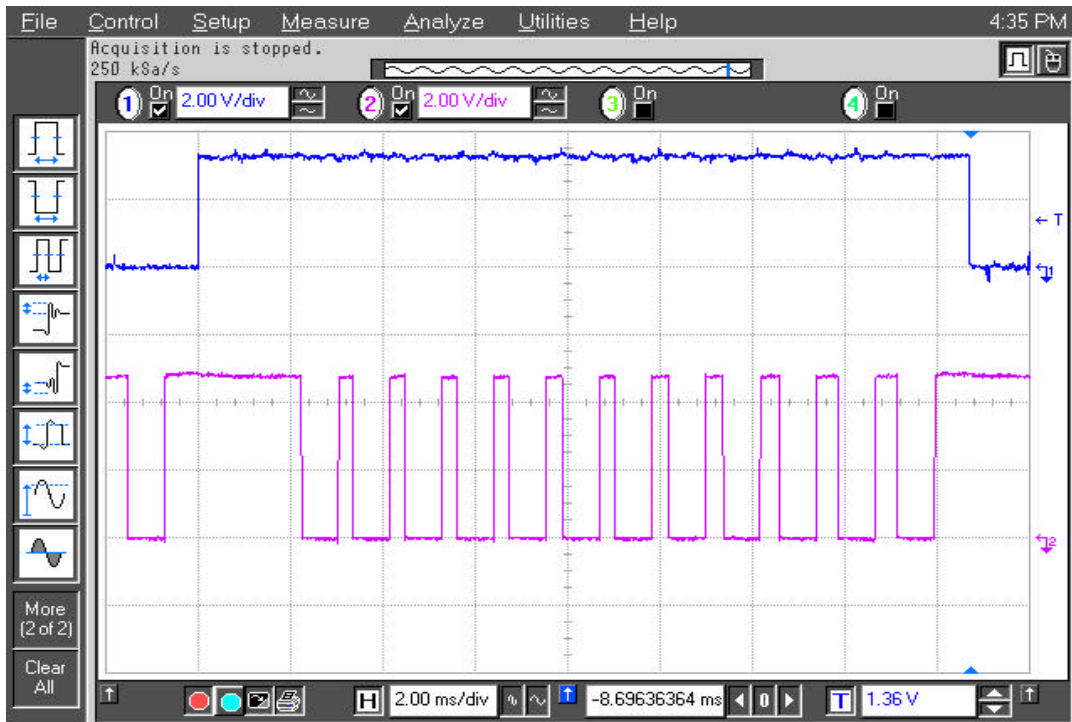
9. Point Probe2 at LY1 pin21 (F2012 pin8 (SIB) on the logic main board) on the jig board.



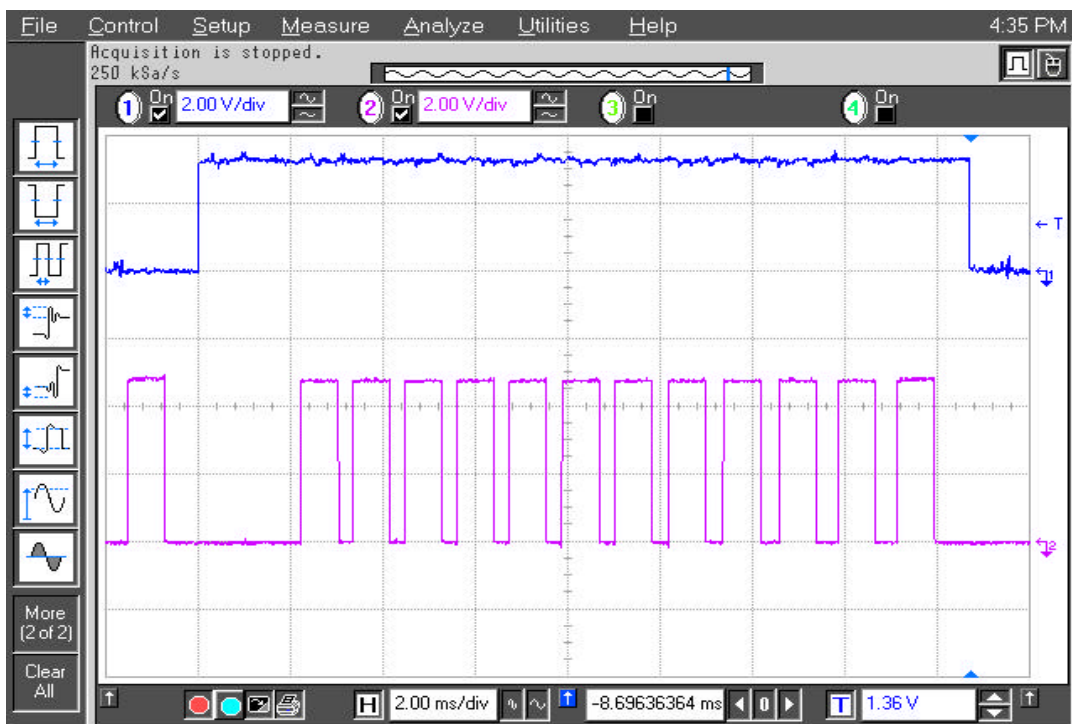
10. Point Probe2 at LY1 pin20 (F2012 pin7 (SIA) on the logic main board) on the jig board.



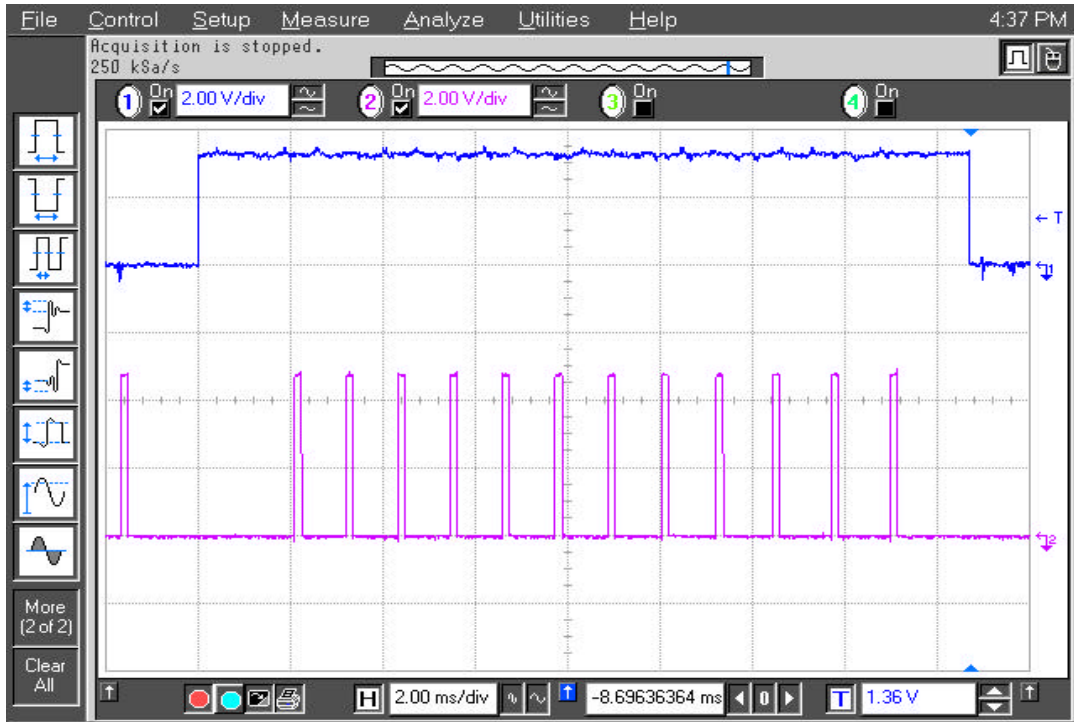
10. Point Probe2 at LY1 pin20 (F2012 pin7 (SIA) on the logic main board) on the jig board.



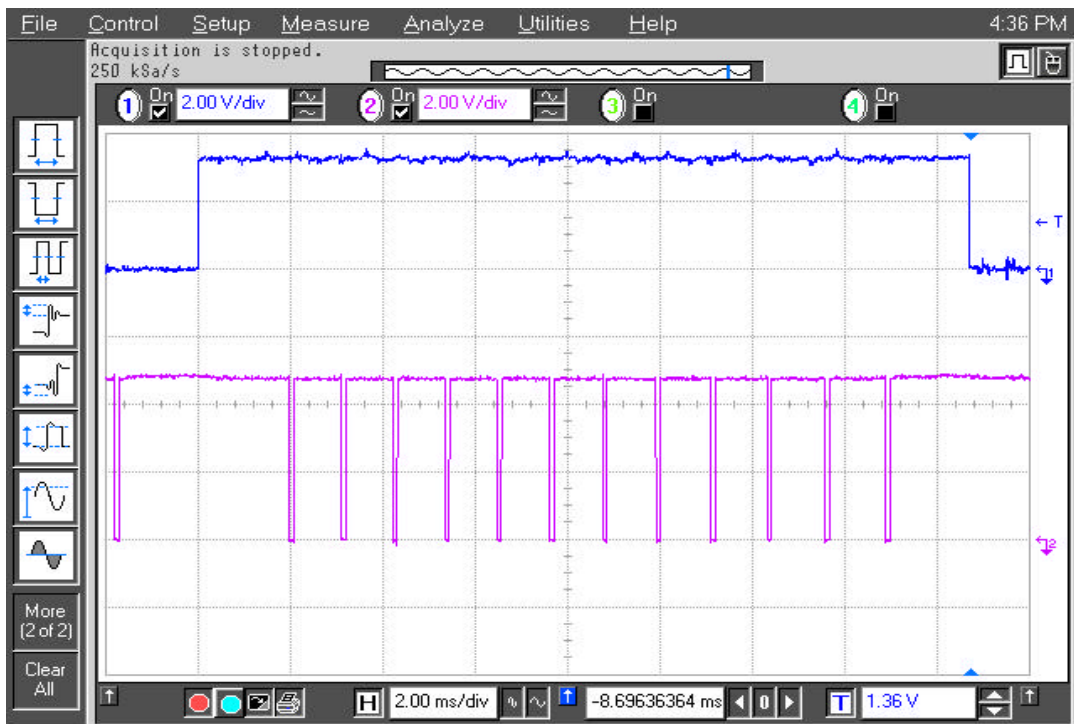
10. Point Probe2 at LY1 pin20 (F2012 pin7 (SIA) on the logic main board) on the jig board.



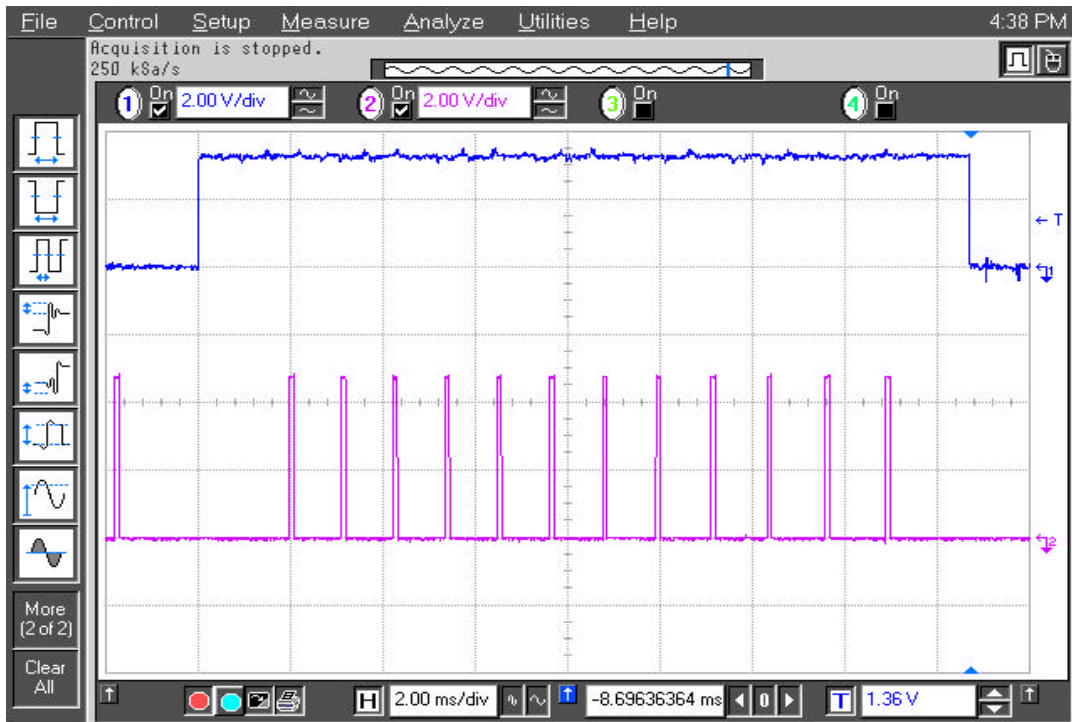
13. Point Probe2 at LY1 pin10 (F2010 pin7 (YFR) on the logic main board) on the jig board.



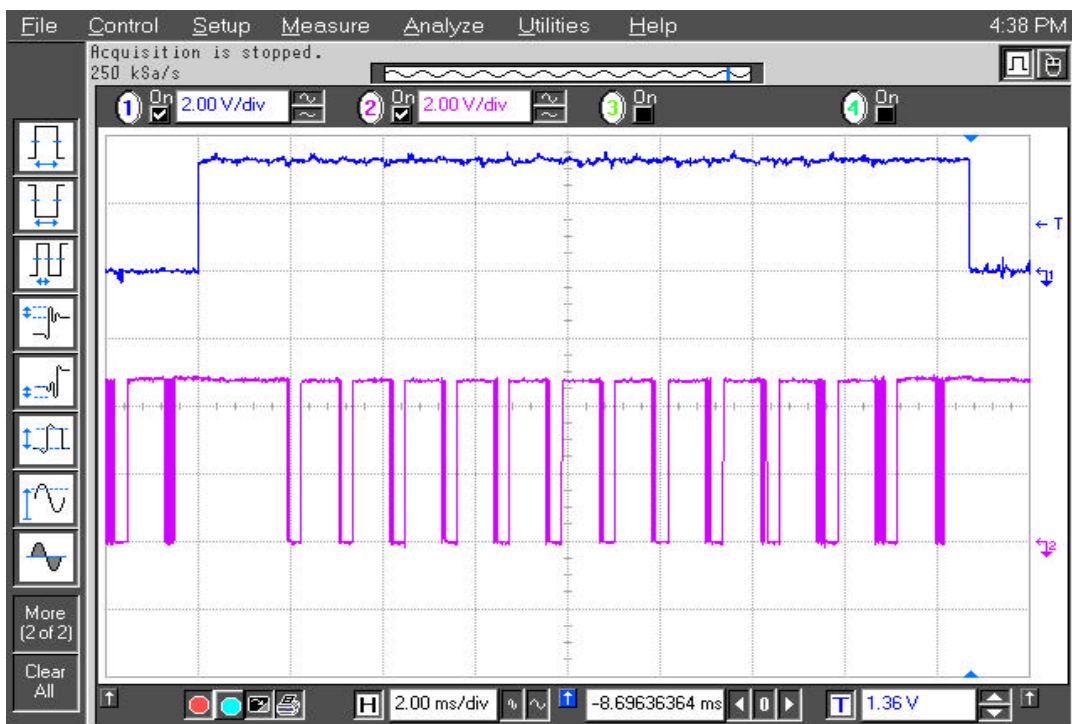
14. Point Probe2 at LY1 pin9 (F2010 pin8 (YP) on the logic main board) on the jig board.



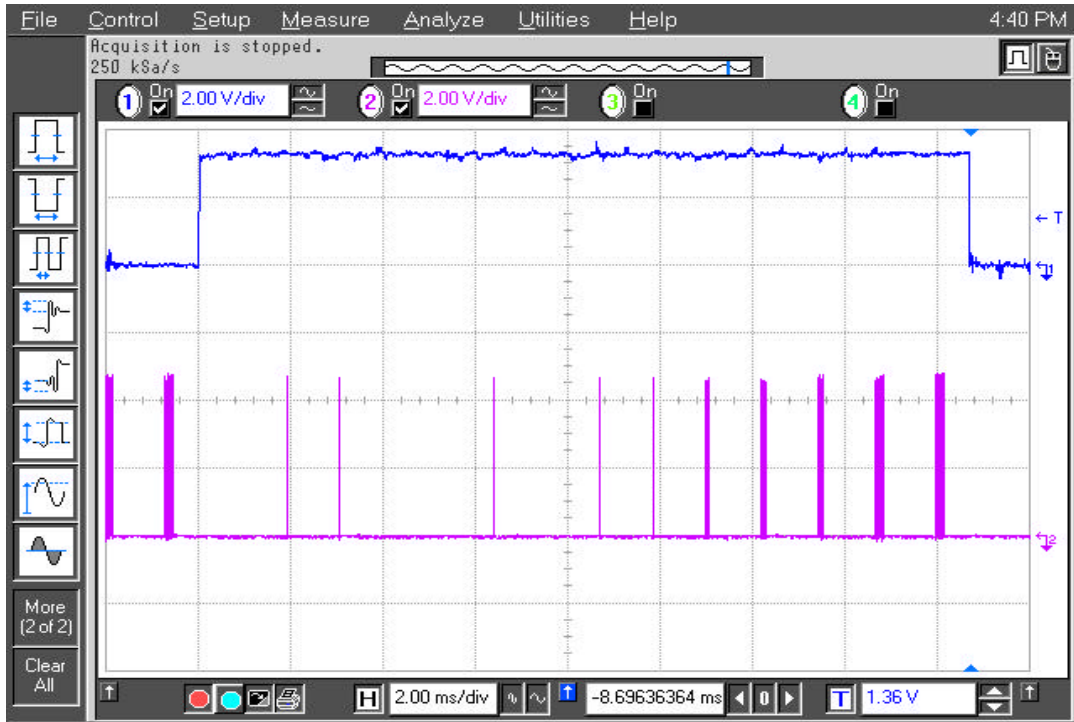
15. Point Probe2 at LY1 pin8 (F2010 pin6 (YRR) on the logic main board) on the jig board.



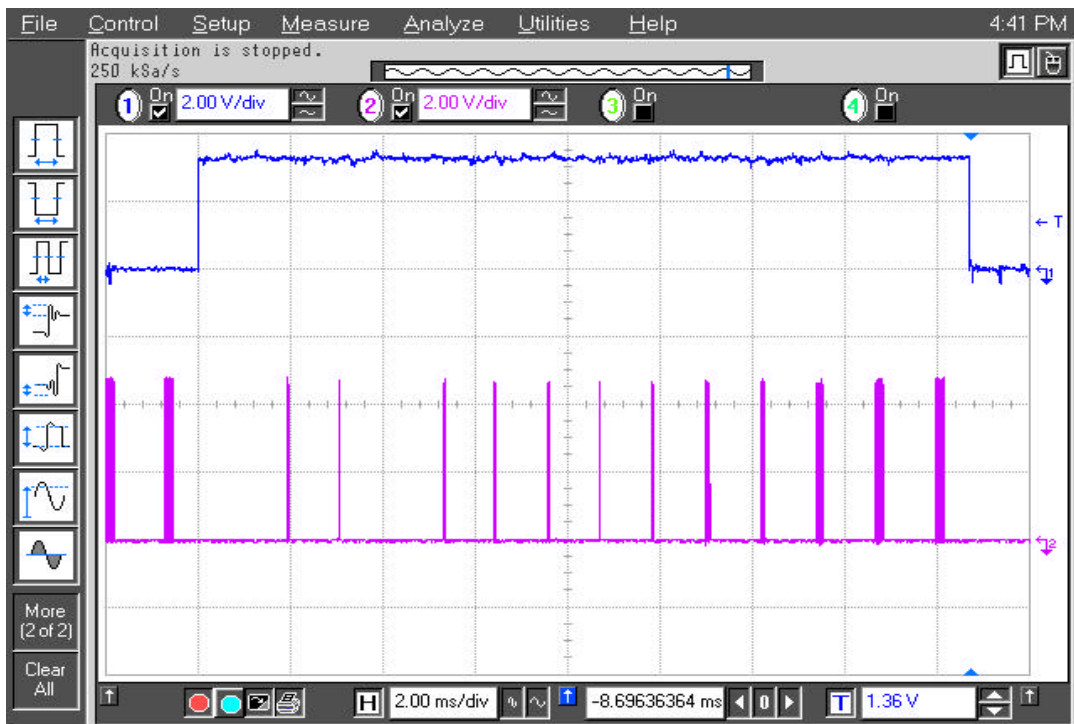
16. Point Probe2 at LY1 pin5 (F2010 pin5 (YG) on the logic main board) on the jig board.



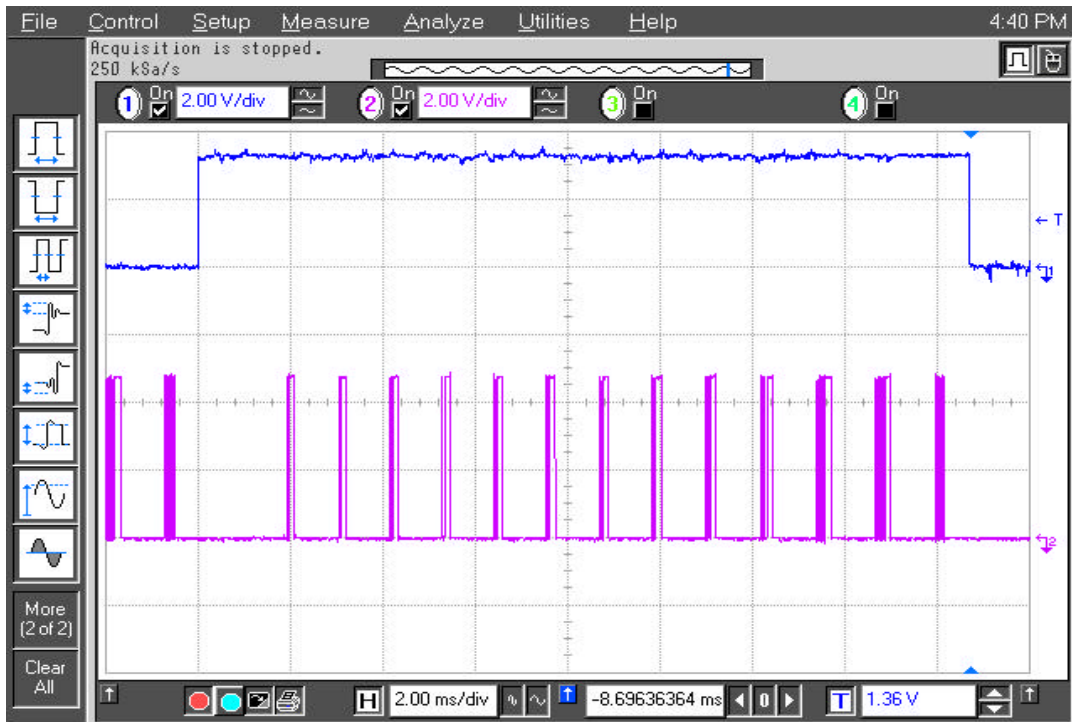
17. Point Probe2 at LY1 pin4 (F2011 pin8 (YF) on the logic main board) on the jig board.



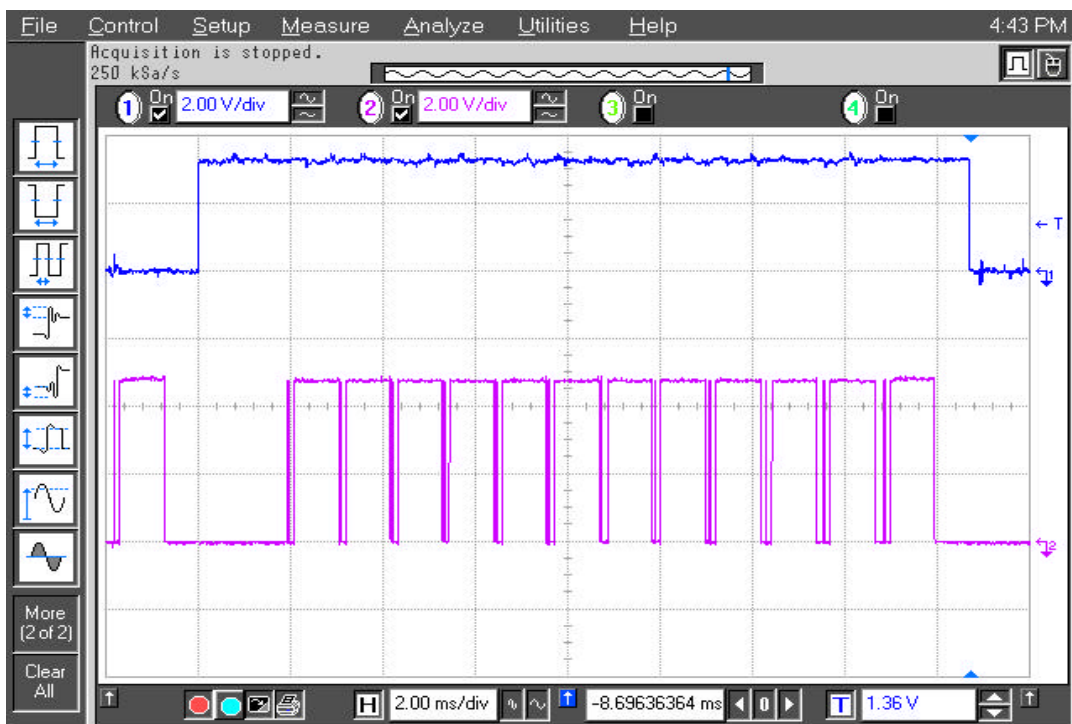
18. Point Probe2 at LY1 pin2 (F2011 pin7 (YR) on the logic main board) on the jig board.



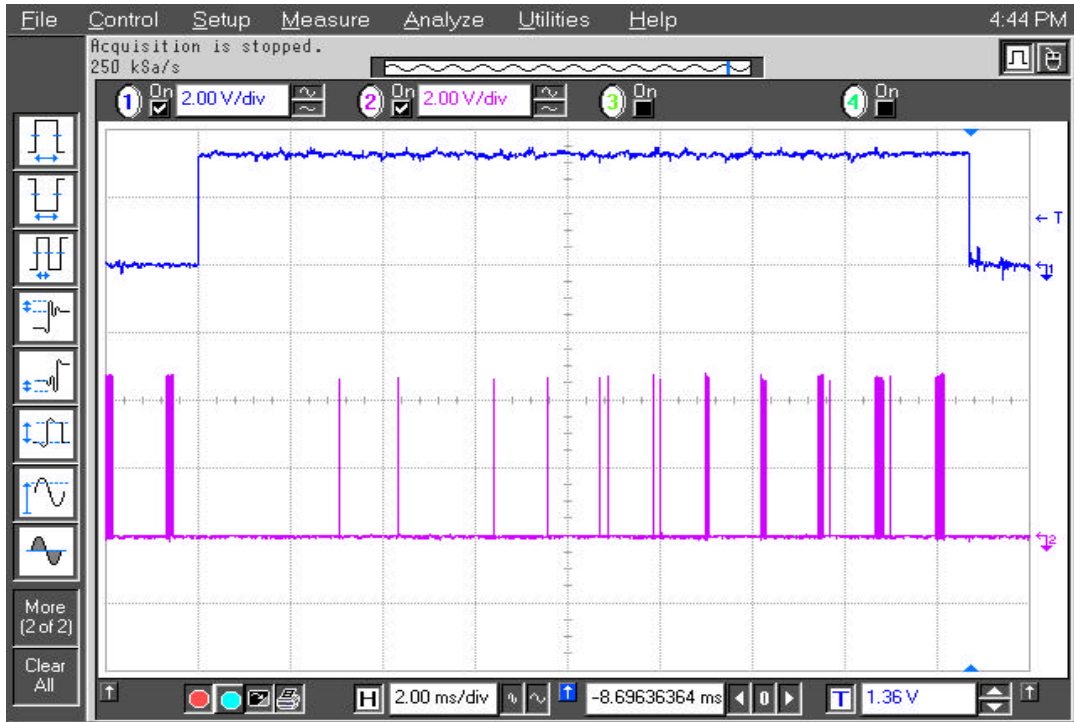
19. Point Probe2 at LY1 pin1 (F2011 pin7 (YS) on the logic main board) on the jig board.



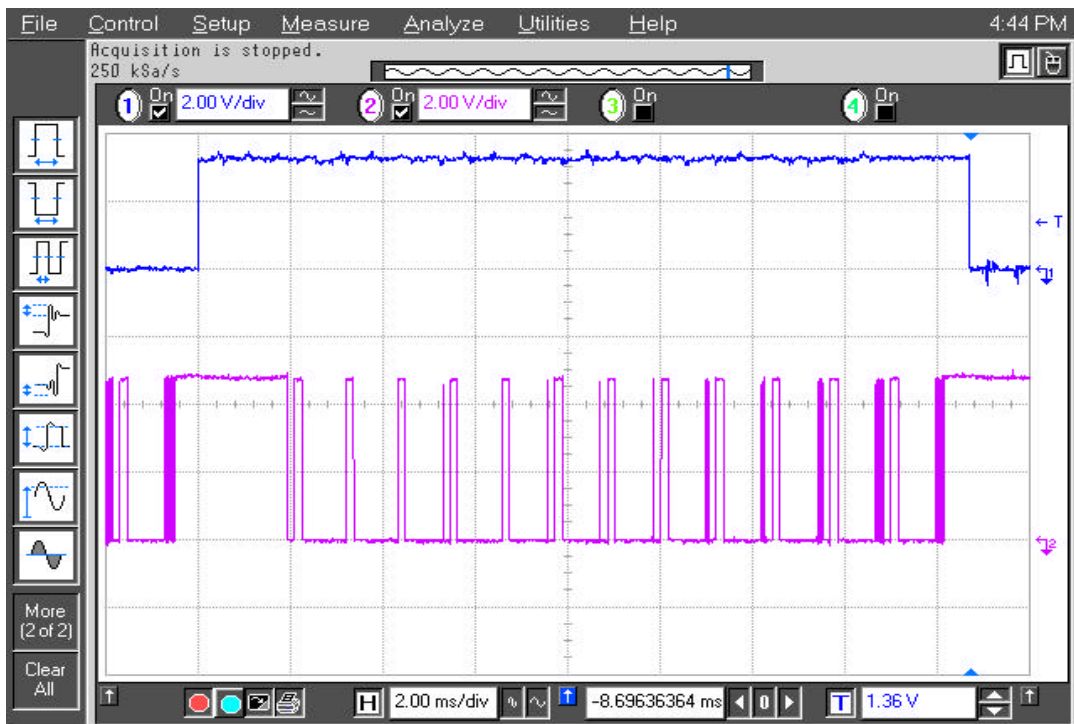
20. Point Probe2 at LX1 pin2 (F2015 pin6 (XRR) on the logic main board) on the jig board.



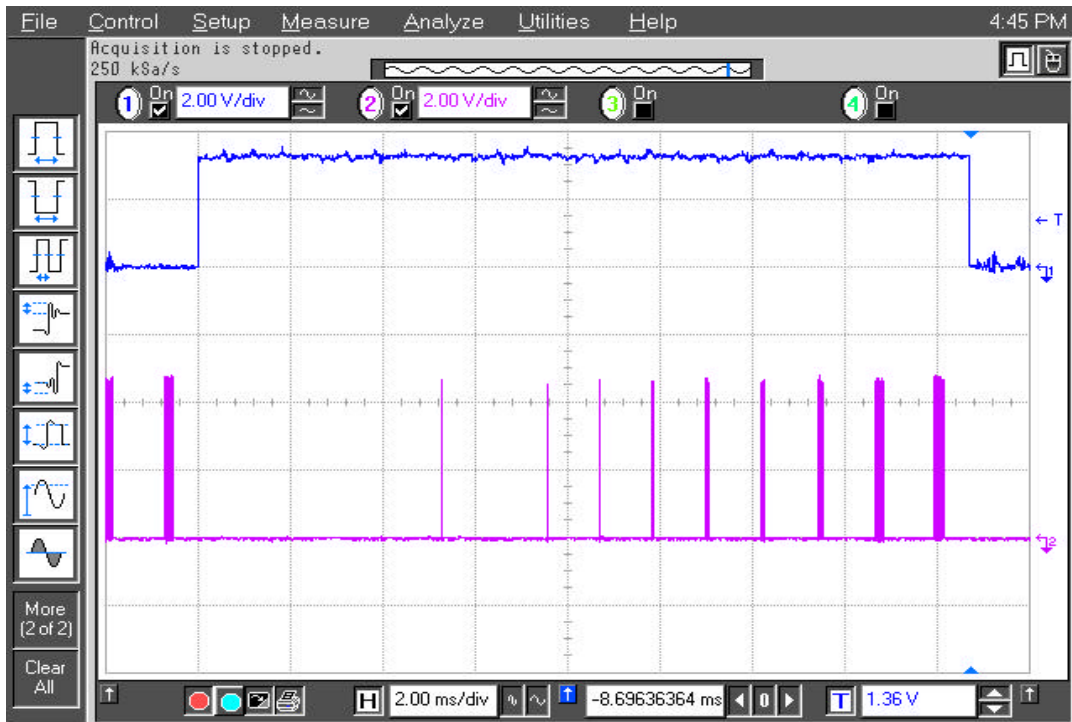
21. Point Probe2 at LX1 pin4 (F2015 pin7 (XR) on the logic main board) on the jig board.



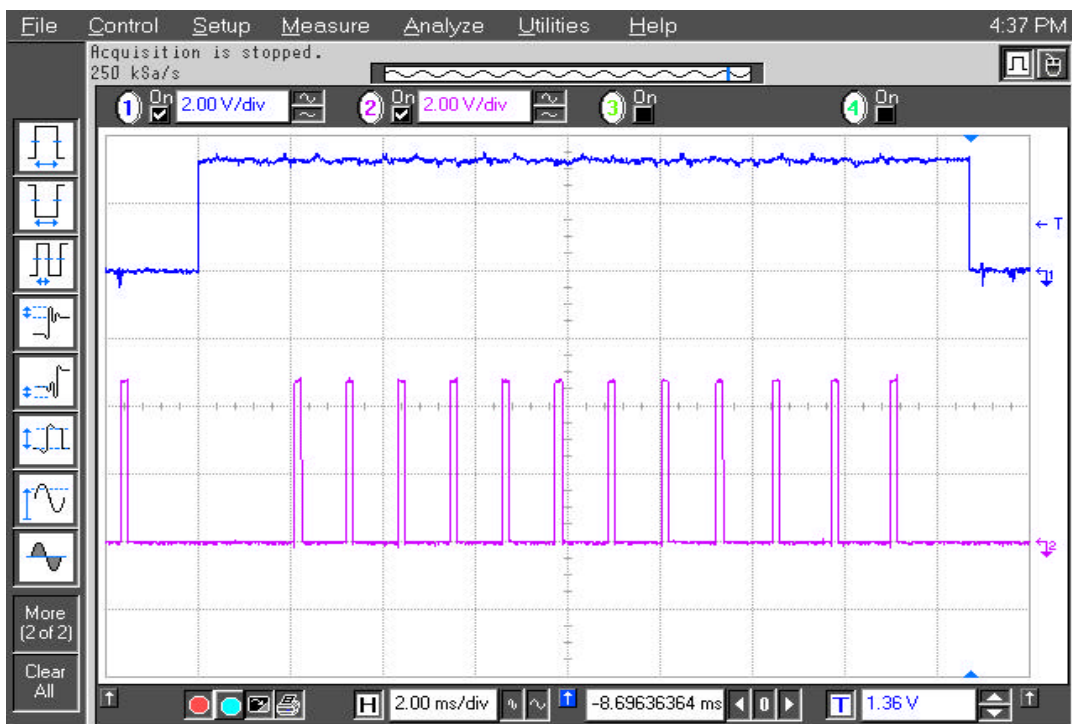
22. Point Probe2 at LX1 pin6 (F2015 pin8 (XS) on the logic main board) on the jig board.



23. Point Probe2 at LX1 pin8 (F2014 pin5 (XF) on the logic main board) on the jig board.

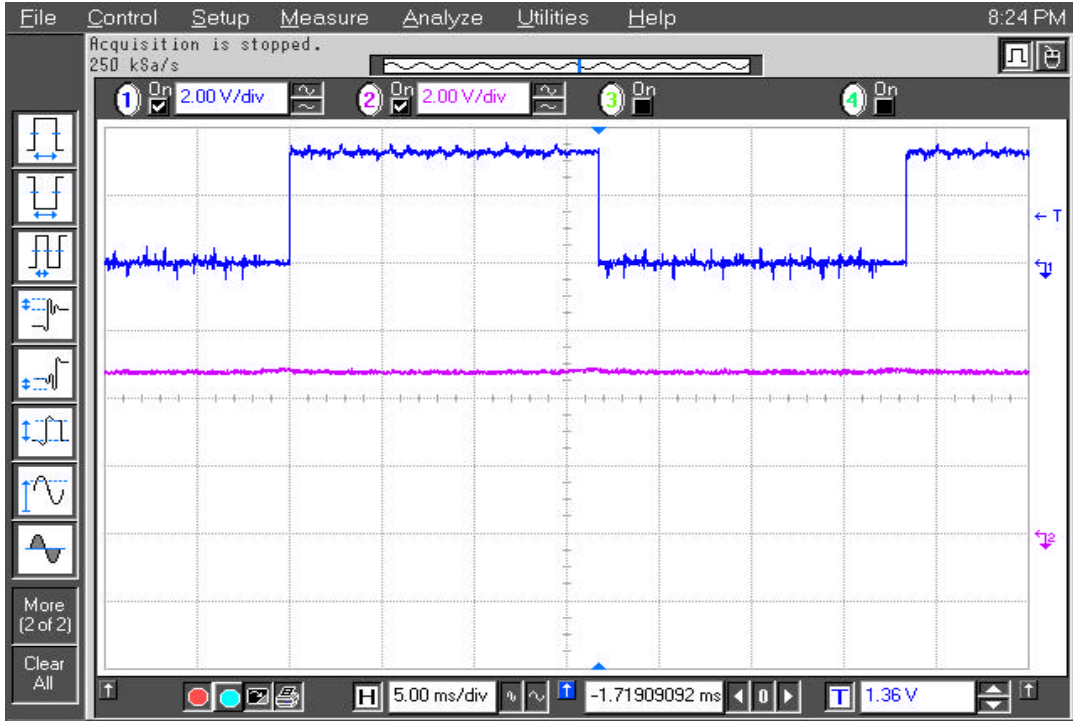


24. Point Probe2 at LX1 pin10 (F2014 pin6 (XG) on the logic main board) on the jig board.



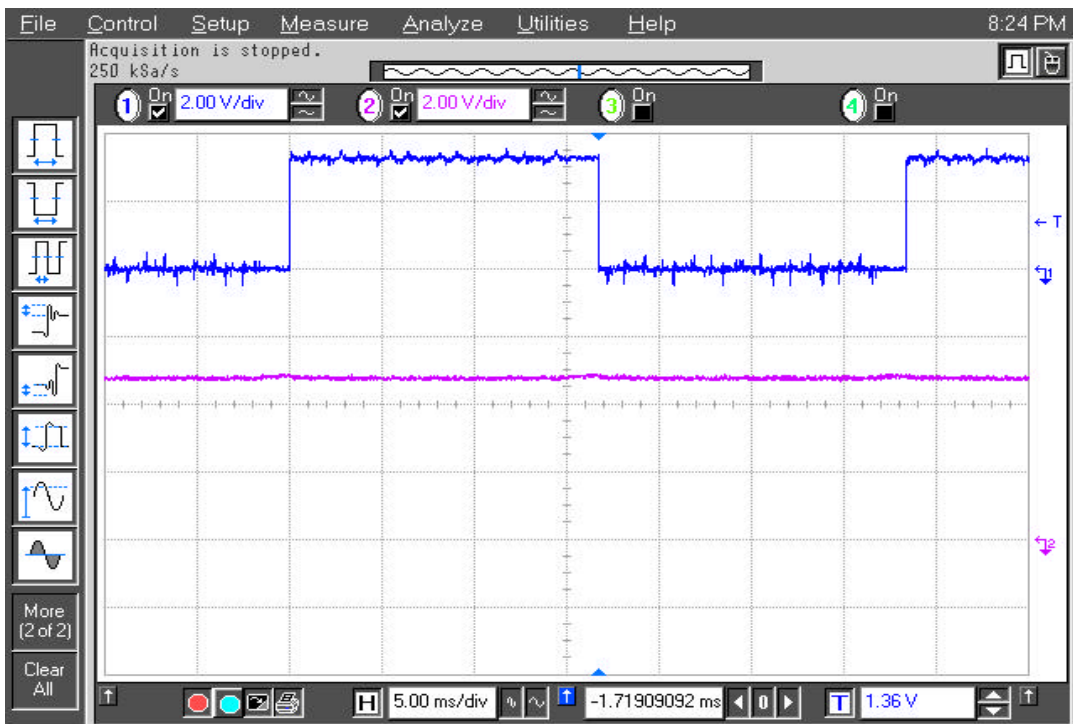
25. Jig board U1 (LE01)

Pins 6 ~ 11, 14 ~ 19, 22 ~ 27, 30 ~ 32, 49 ~ 51, 54 ~ 59, 62 ~ 67, 70 ~ 75

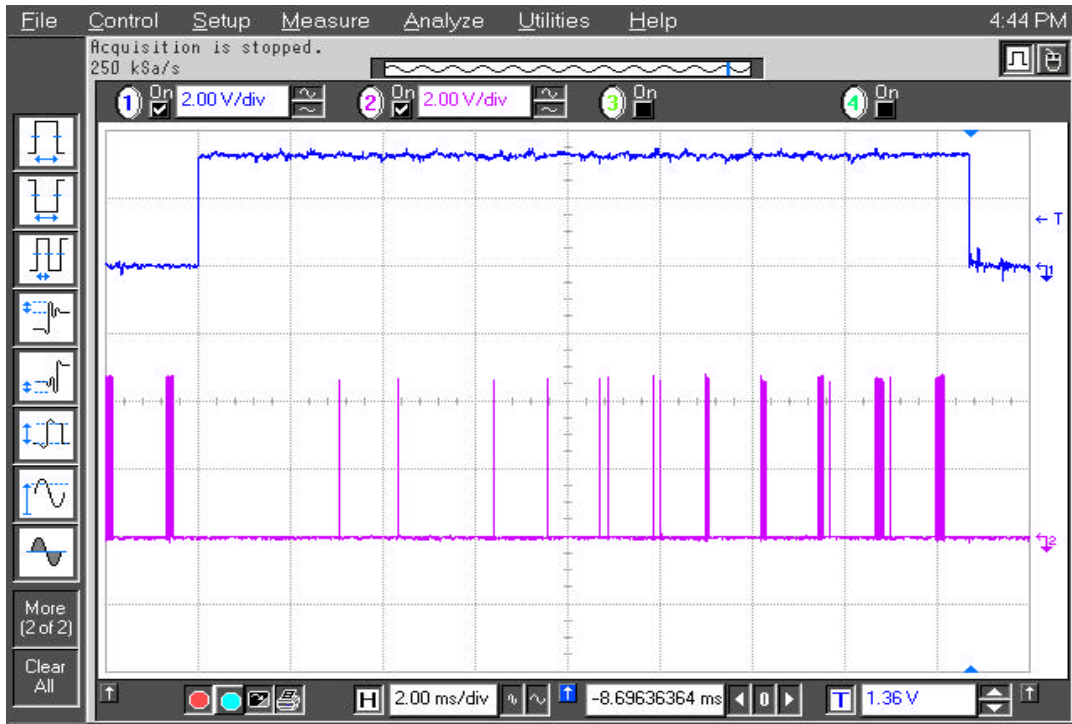


26. Jig board U2 (LE02)

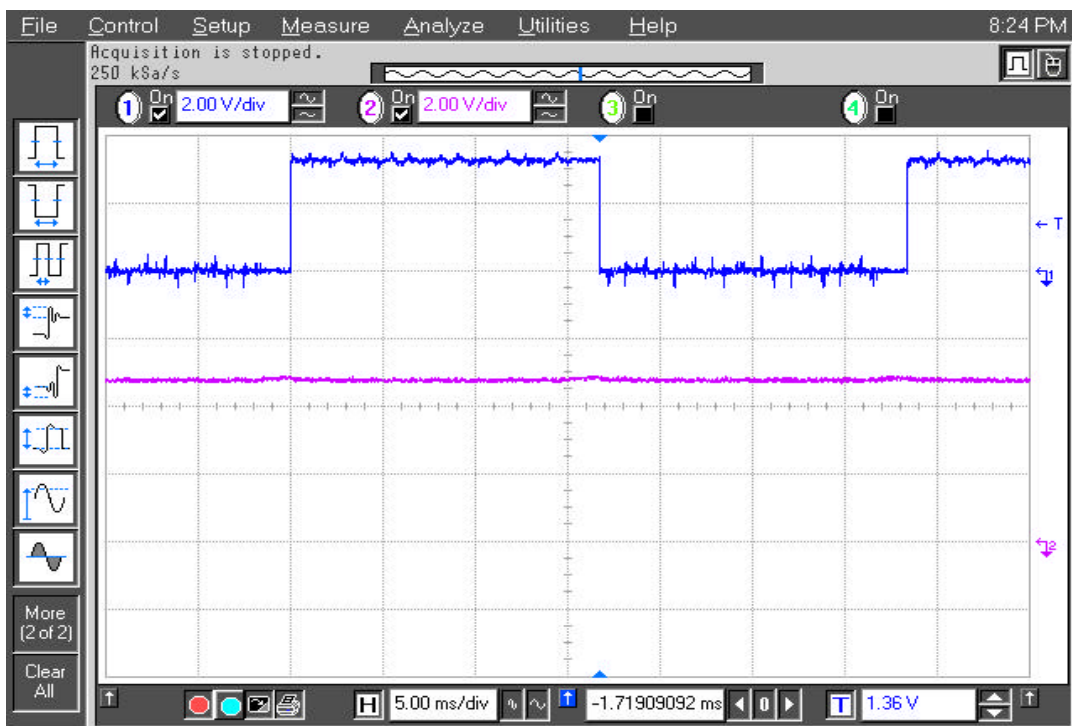
Pins 6 ~ 11, 14 ~ 19, 22 ~ 27, 30 ~ 32, 49 ~ 51, 54 ~ 59, 62 ~ 67, 70 ~ 75



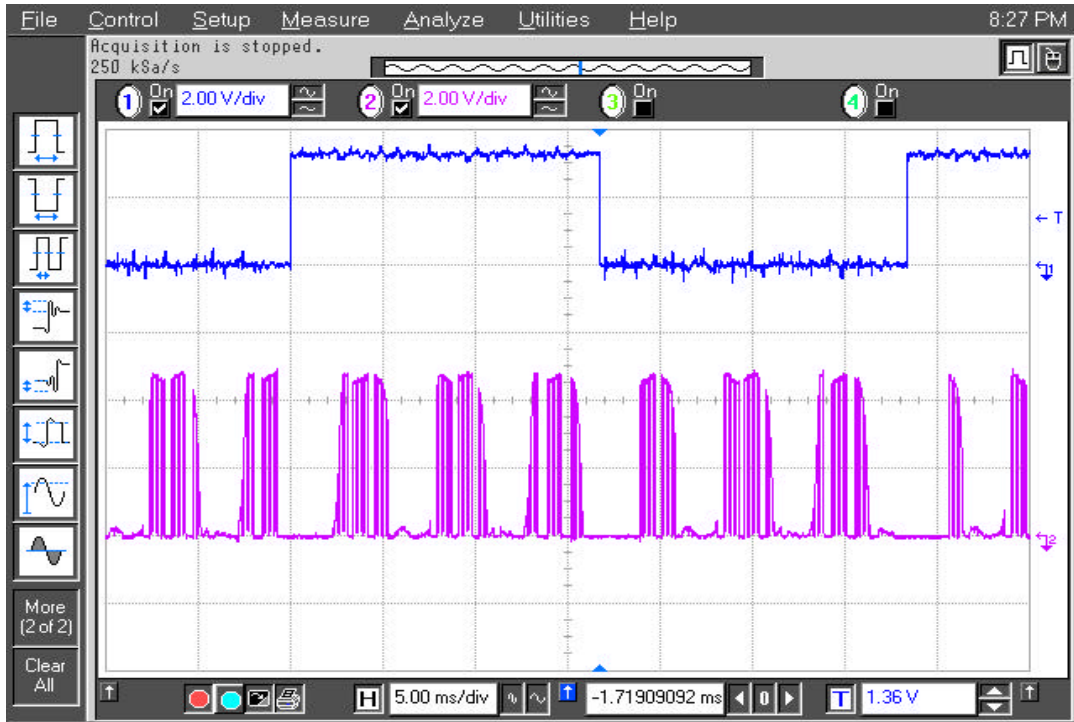
27. Jig board U1 (LE01)
Pins 39, 40, 41, 42



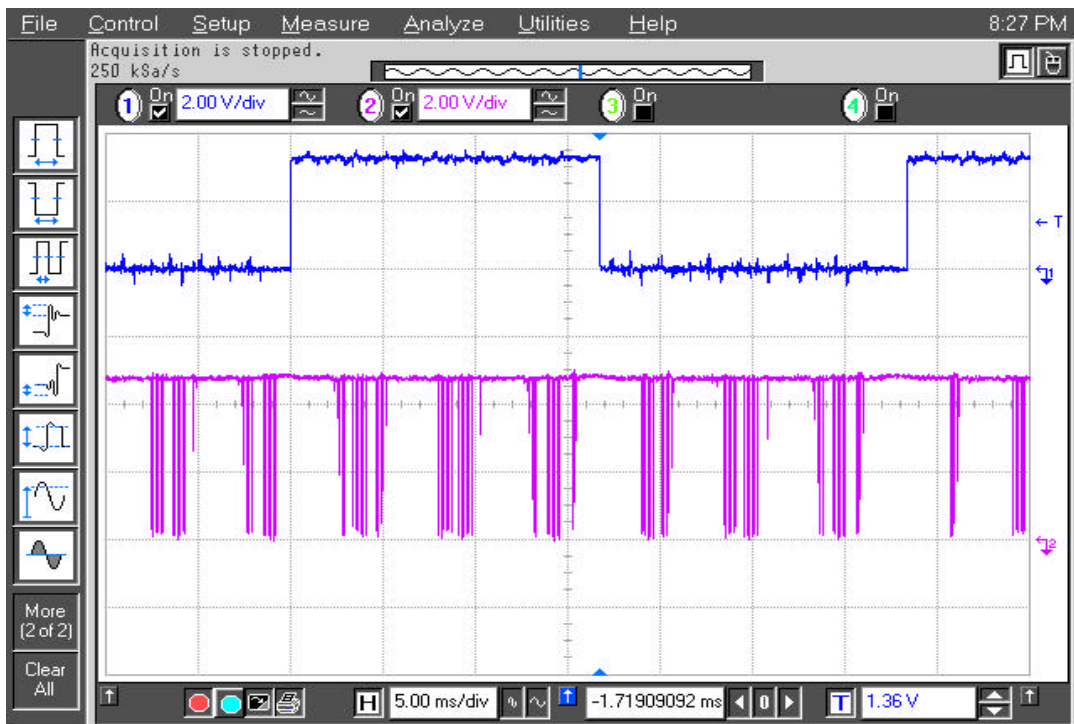
28. Jig board U2 (LE02)
Pins 39, 40, 41, 42



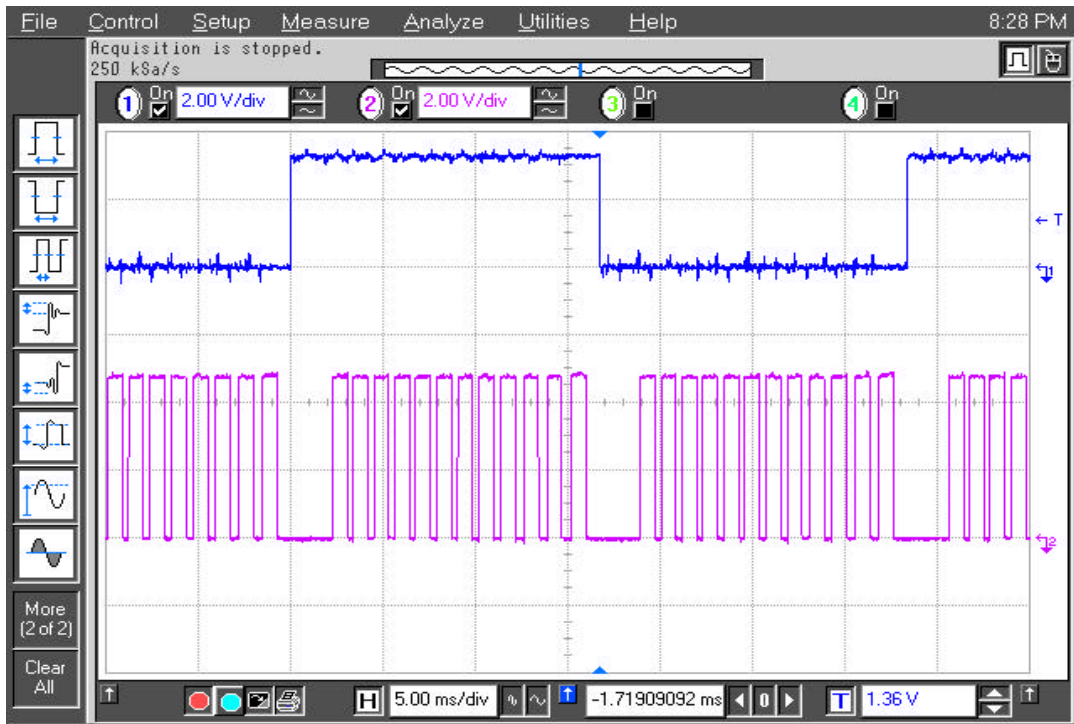
29. Jig board U1 (LE01) pin35



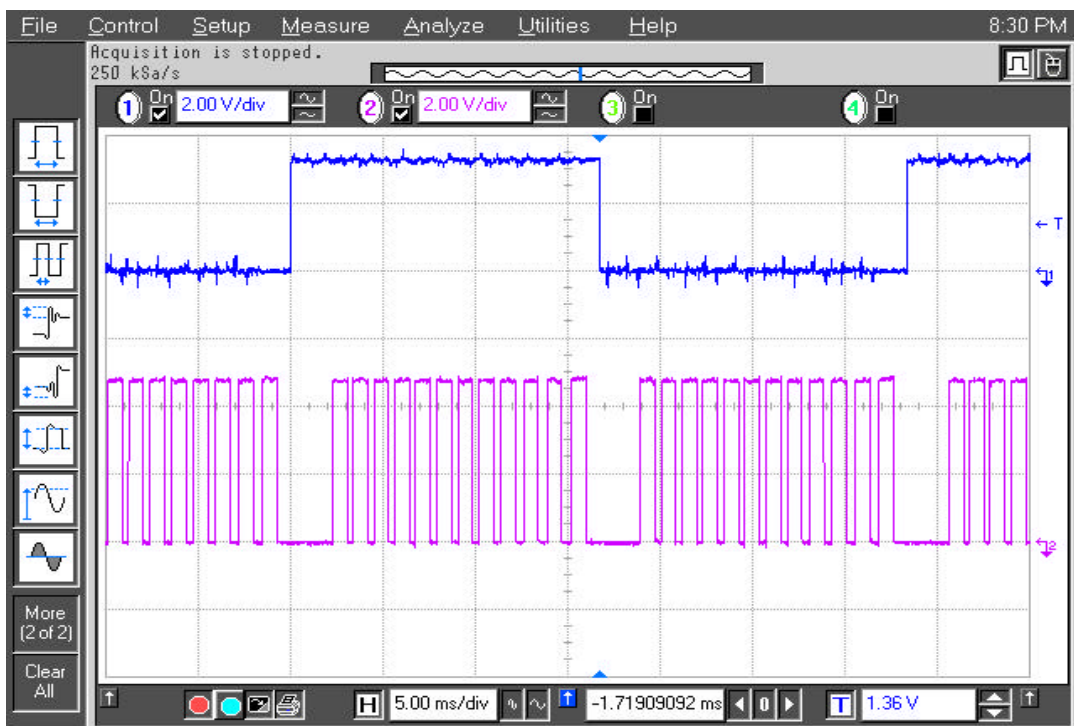
30. Jig board U1 (LE01) pin46



31. Jig board U2 (LE02) pin35

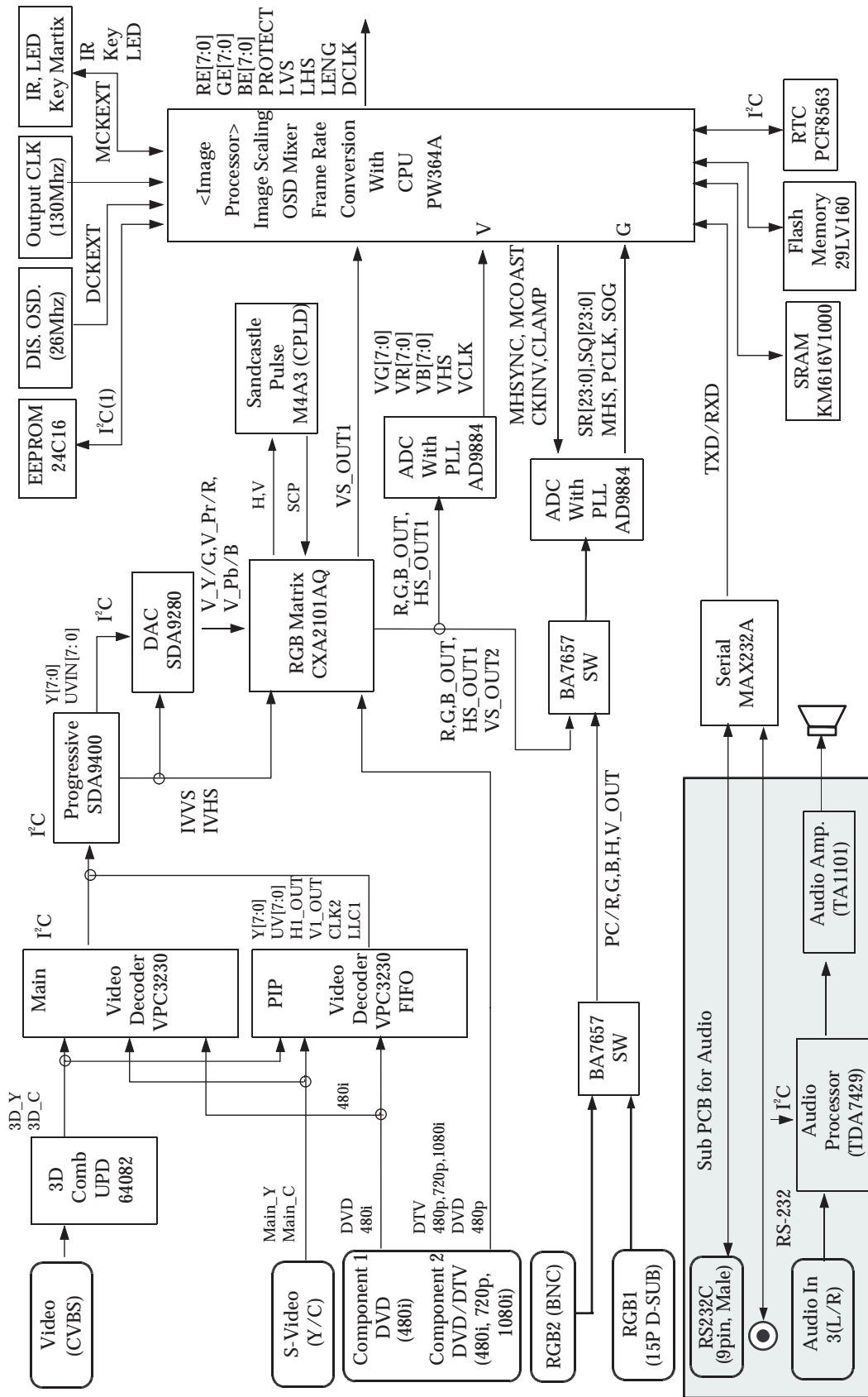


32. Jig board U2 (LE02) pin46



5-4 Block Diagram

5-4-1 42" Monitor Scaler Block Diagram



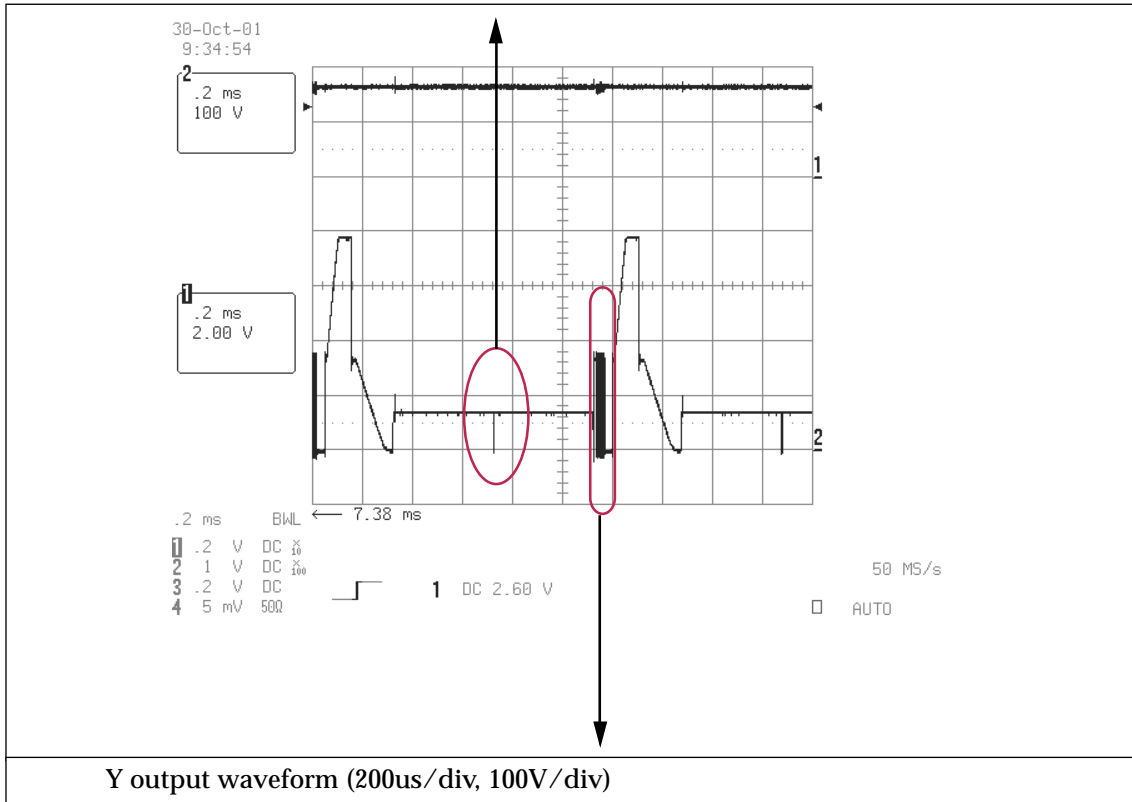
5-5 Major In/Out Signal Waveforms and Voltages of the Unit

5-5-1 In/Out Waveforms

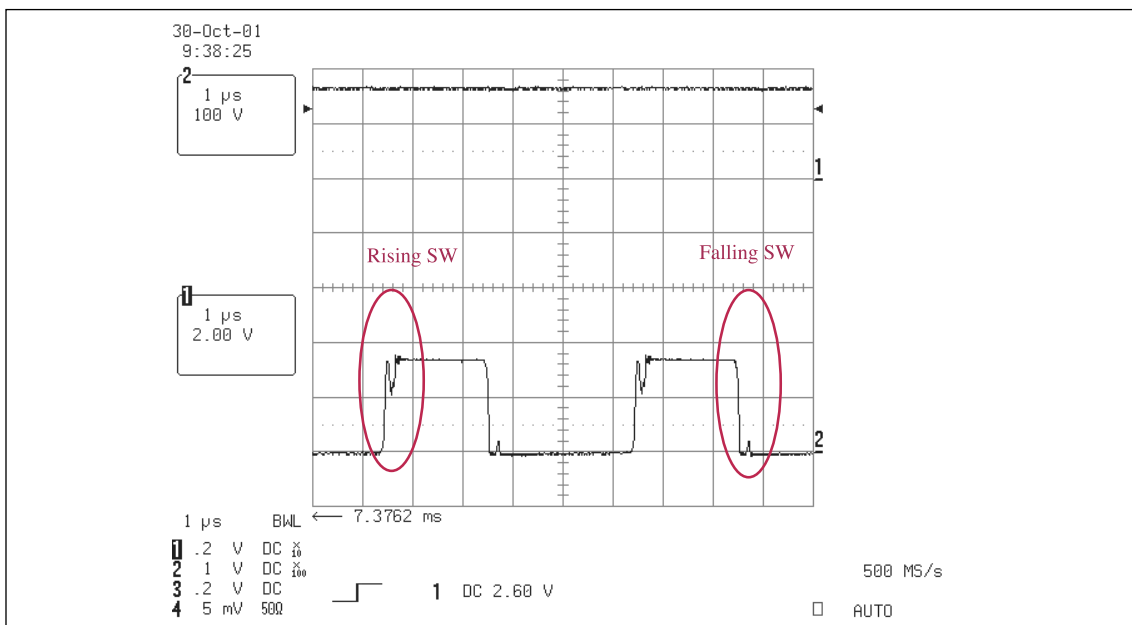
r Y output waveform

- It is the waveform when it is not connected to the panel.

* You should check that a single scan waveform is outputted!!!

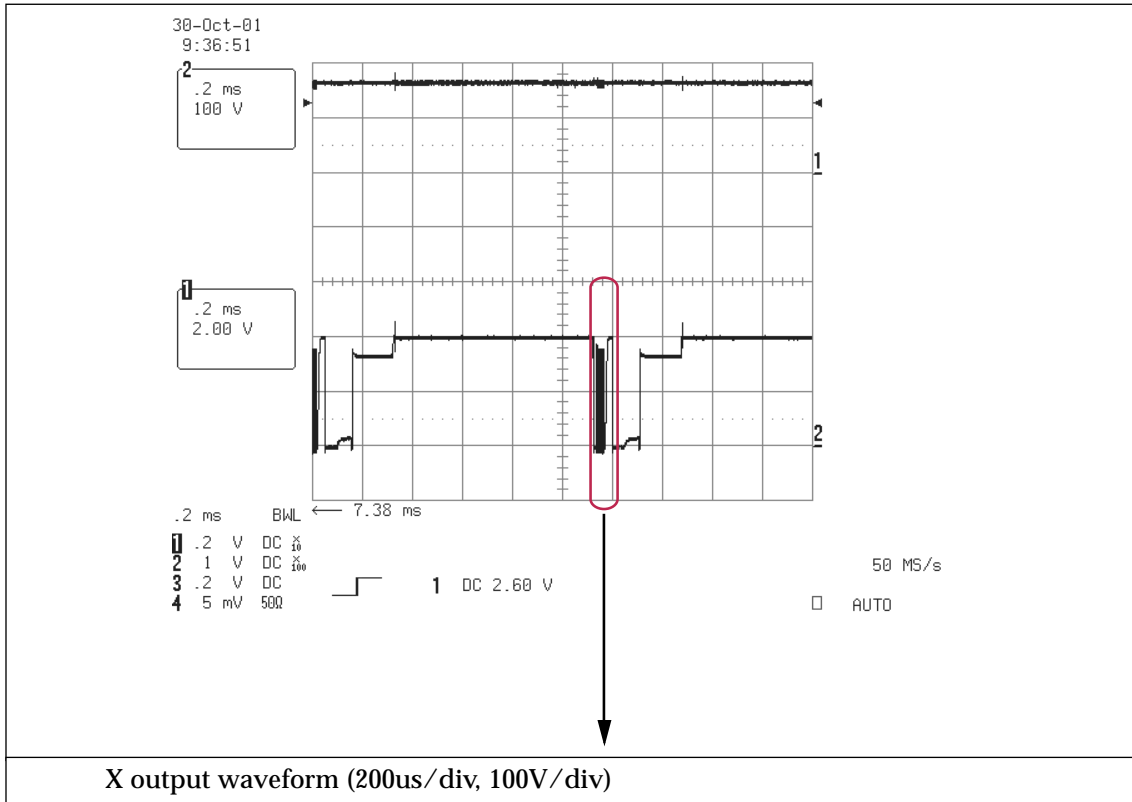


* You should check that energy recovery software is in operation!!!

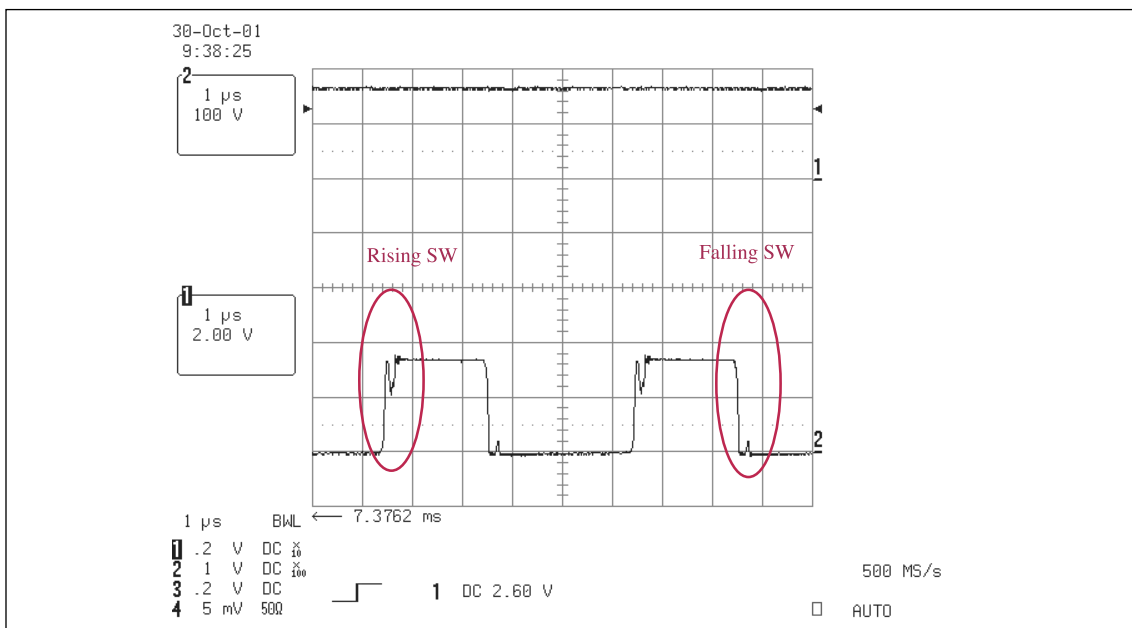


r X output waveform

- It is the waveform when it is not connected to the panel.

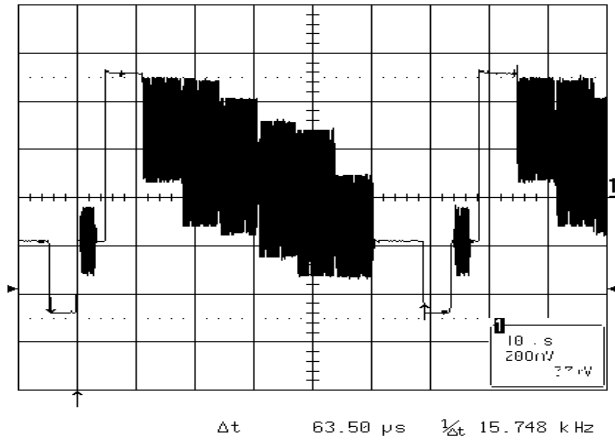


* You should check that energy recovery software is in operation!!!

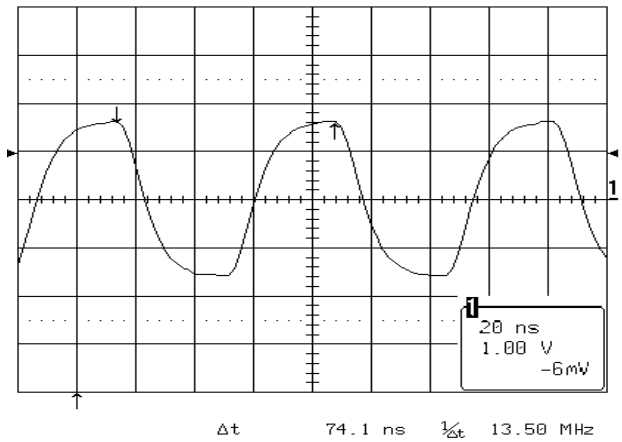


5-6 Main I/O signal pulses and voltages

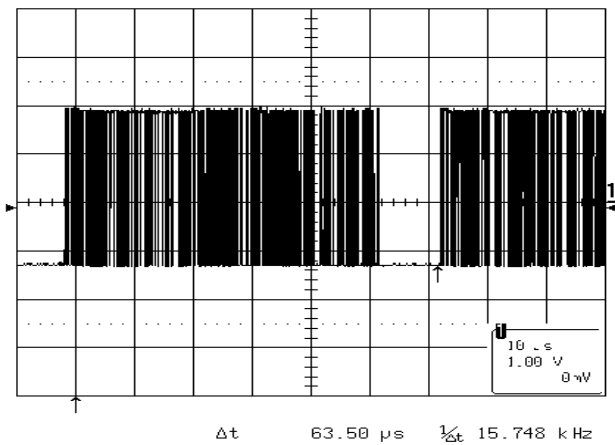
5-6-1 Signal Pulses of Image Board(Input Signal Conditions : 7 Color bar)



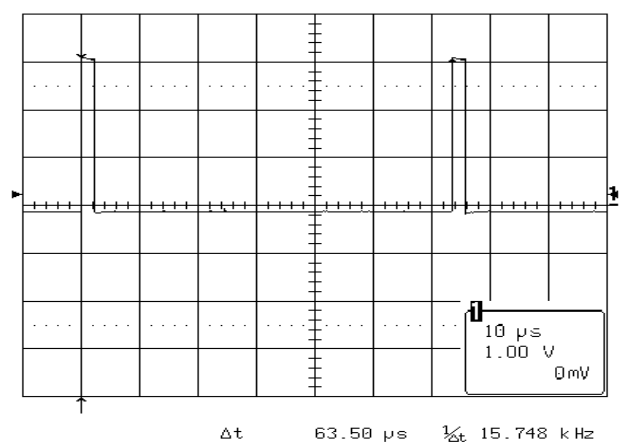
* C203 VIDEO INPUT(CVBS Input)



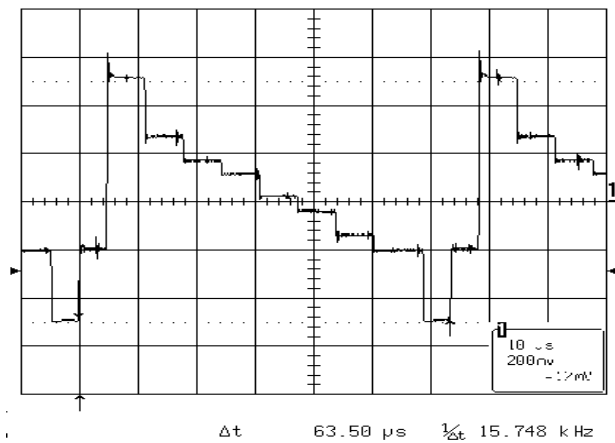
* IC201(VPC3230 MAIN) PIN28 LLC1_OUT



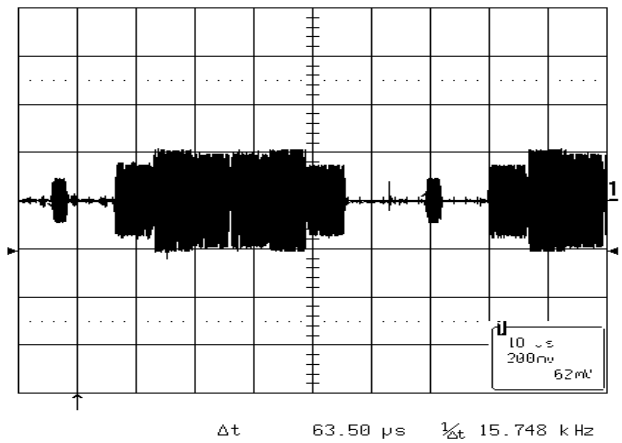
* IC201(VPC3230 MAIN) PIN40 Yo_OUT



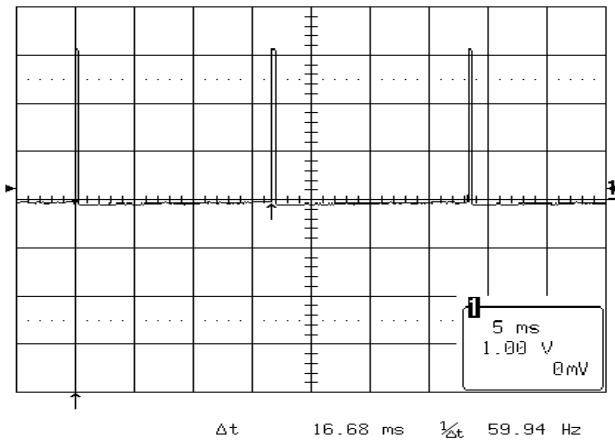
* IC201(VPC3230 MAIN) PIN56 HS_OUT



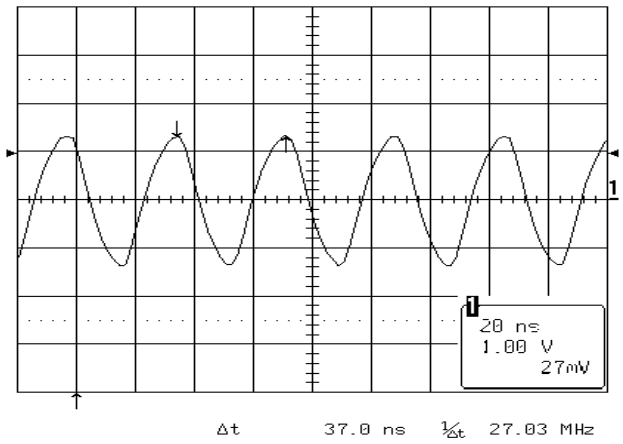
* IC201(VPC3230 MAIN) PIN74 Y_IN



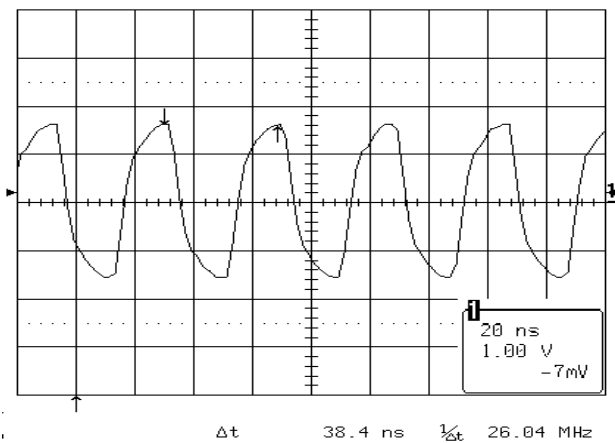
* IC201(VPC3230 MAIN) PIN72 C_IN



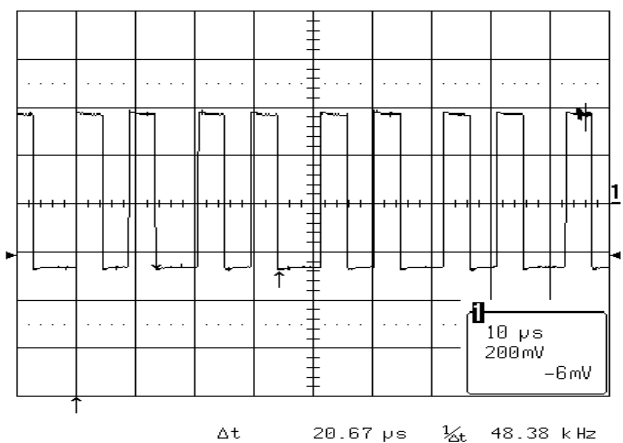
* IC201 (VPC3230 MAIN) PIN57 VS_OUT



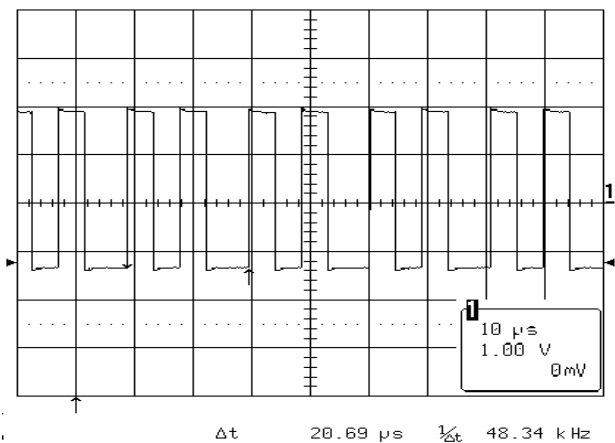
* IC201 (VPC3230 MAIN) PIN27 LLC2_OUT



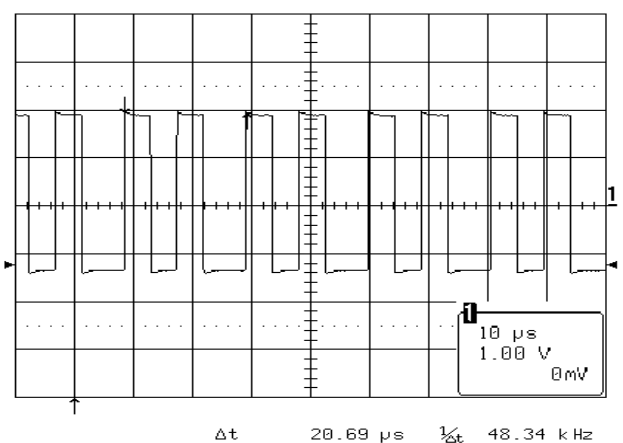
* IC301(PW364A) PIN:AD13 DCLK_OUT



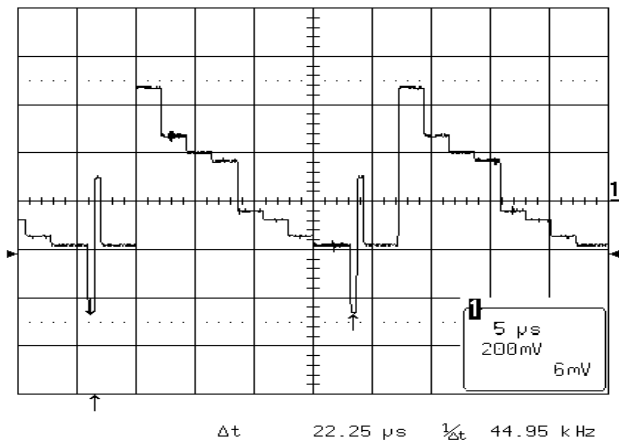
* IC801(AD9884) PIN7 R_IN



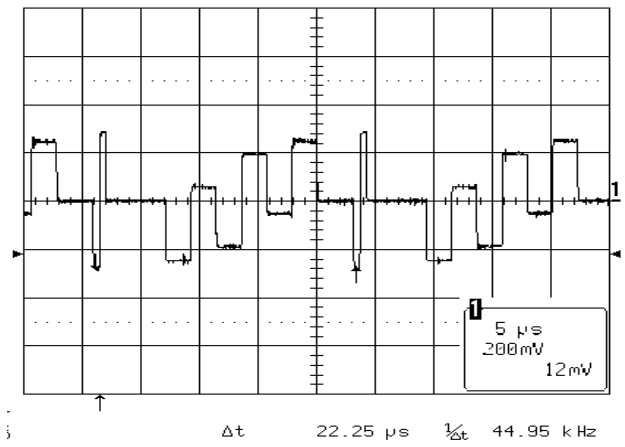
* IC801(AD9884) PIN95 ROUT_ODD



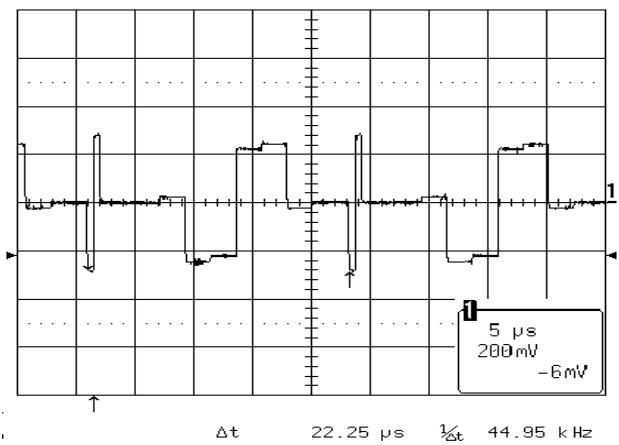
* IC801(AD9884) PIN105 ROUT_EVEN



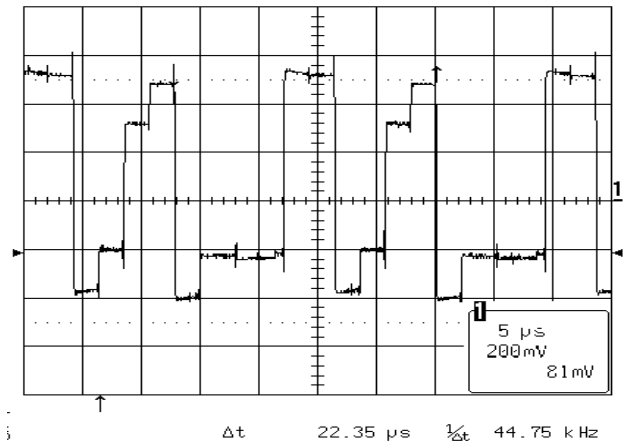
* IC402(CXA2101AQ) PIN5 DTV.Y_IN



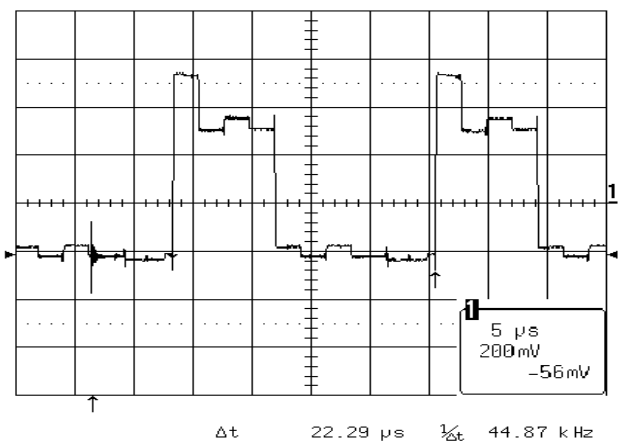
* IC402(CXA2101AQ) PIN4 DTV.Pb_IN



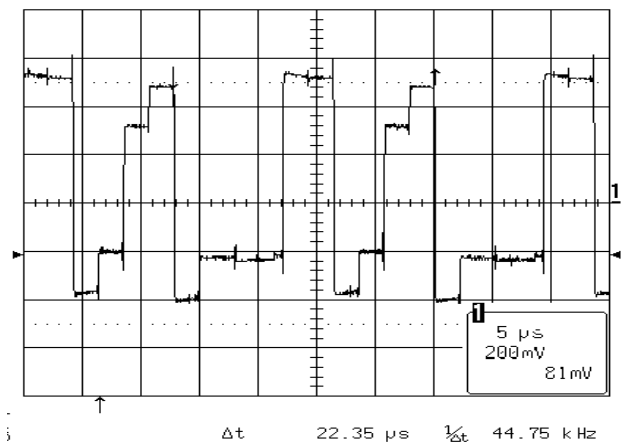
* IC402(CXA2101AQ) PIN3 DTV.Pr_IN



* IC402(CXA2101AQ) PIN35 DTV.R_OUT



* IC402(CXA2101AQ) PIN37 DTV.G_OUT

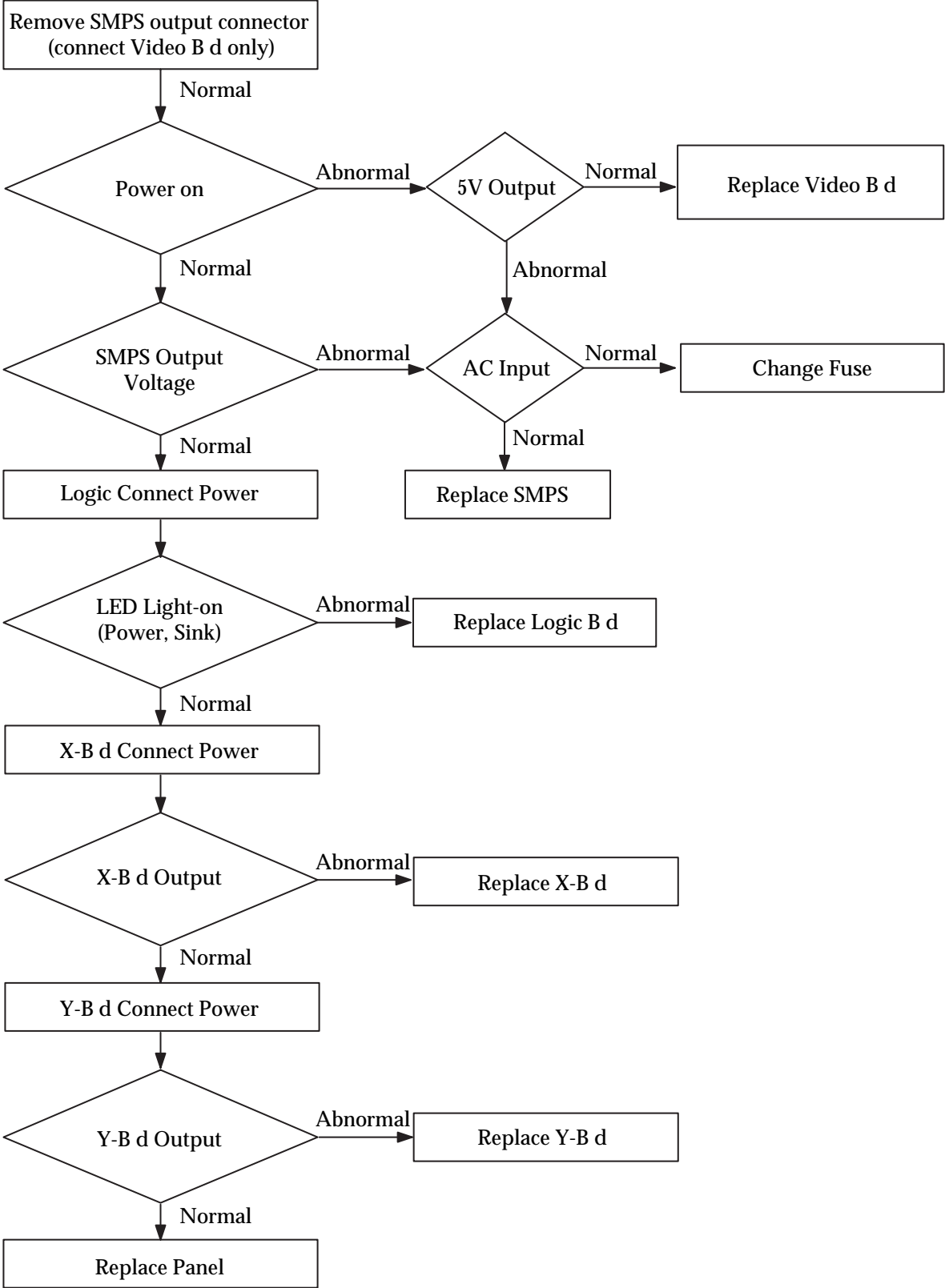


* IC402(CXA2101AQ) PIN39 DTV.B_OUT

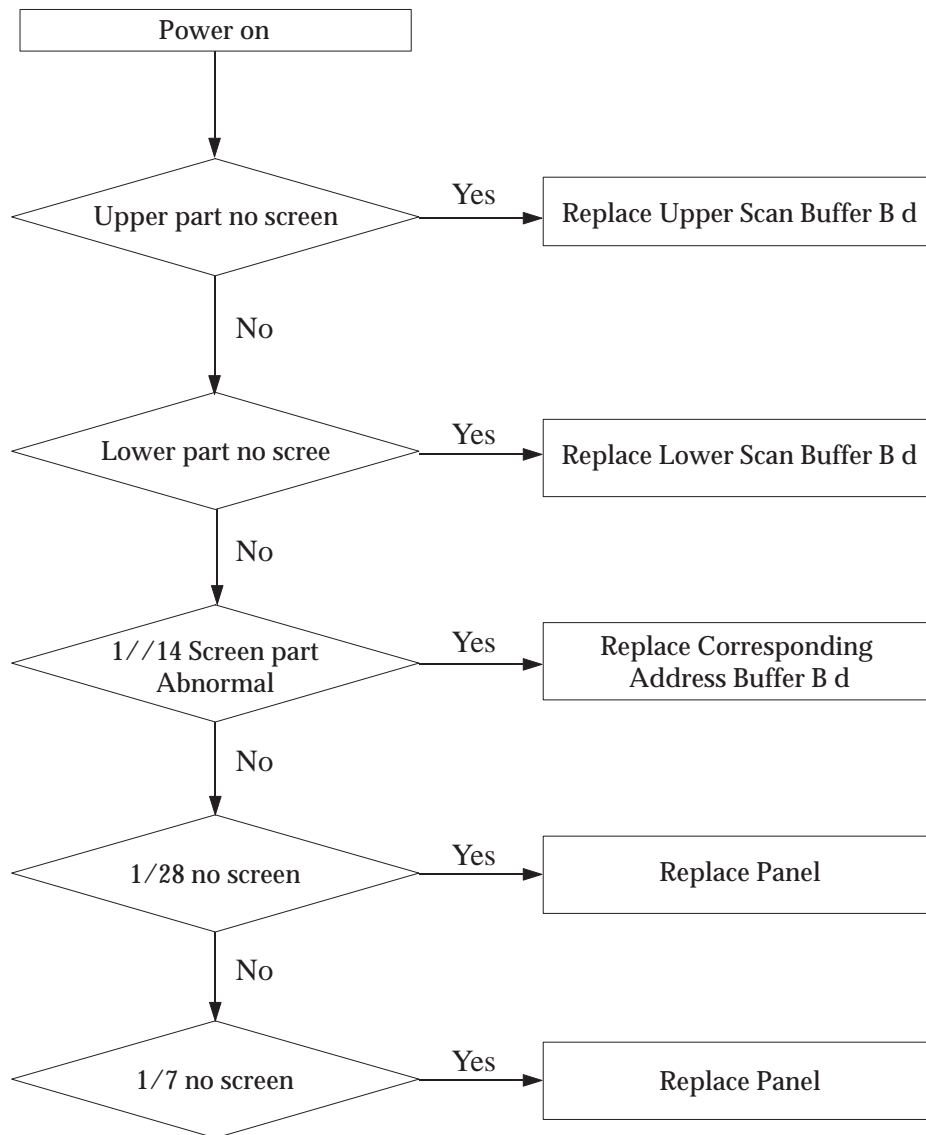
MEMO

6. Troubleshooting

6-1 Entirely no screen



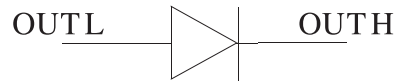
6-2 Partly no screen



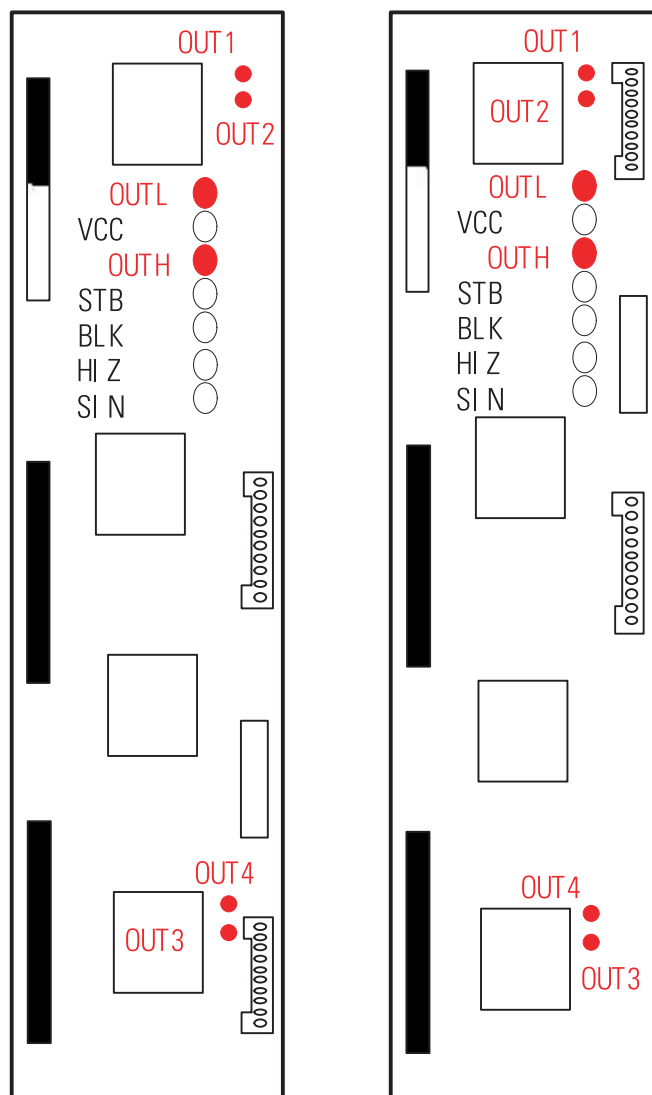
6-3 Checking the Board (Unit)

6-3-1 Y buffer

- To check the main board, you have to check the Y buffer first.
- After separating Y Main and Y buffer board,
- Check the Diode between OUTL and OUTH, and make sure that the forward voltage drop is between 0.4 and 0.5V.

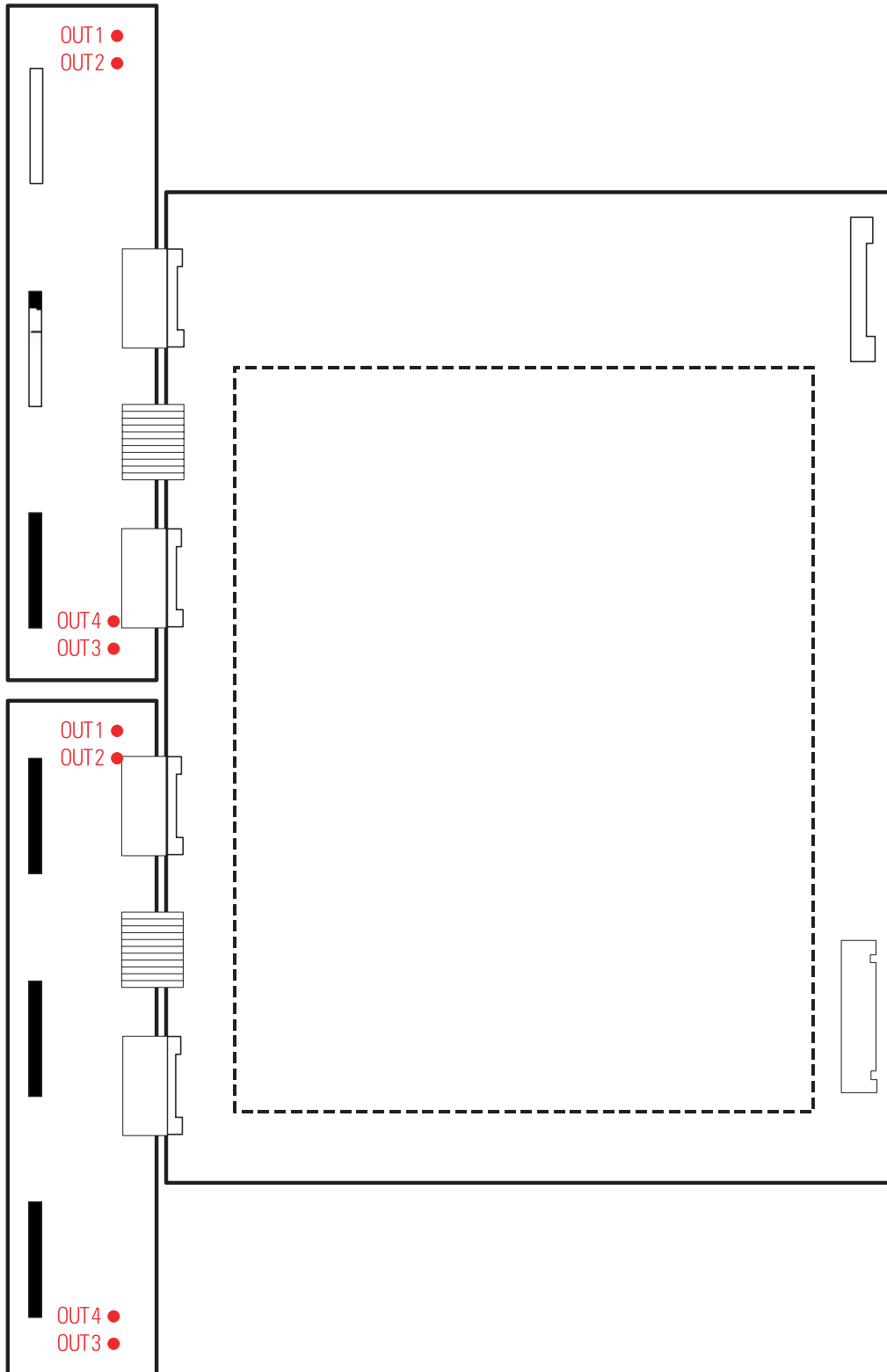


- Check that the resistance between the two terminals is more than several kW.



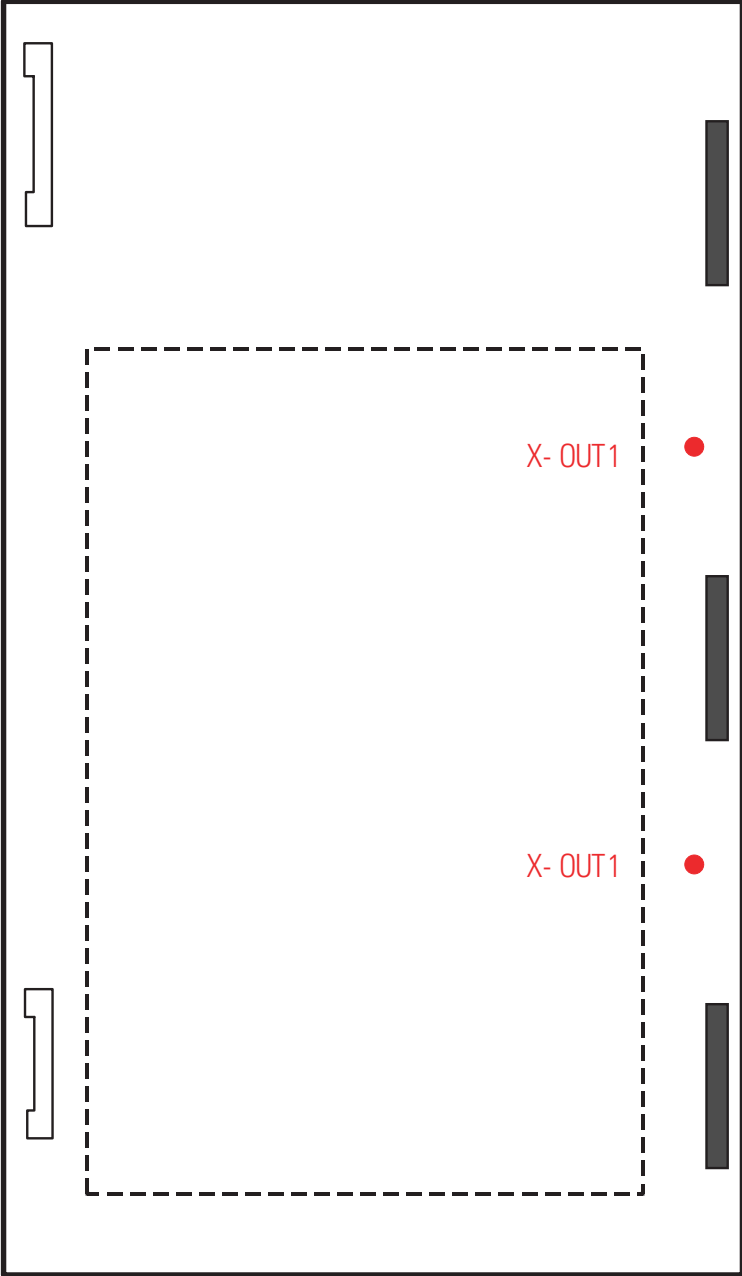
6-3-2 Y Main

- After connecting Y main and Y buffer board, check that one of the output waveforms from OUT 1, 2, 3 or 4 is the same as that of the appendix 1 when power is supplied.



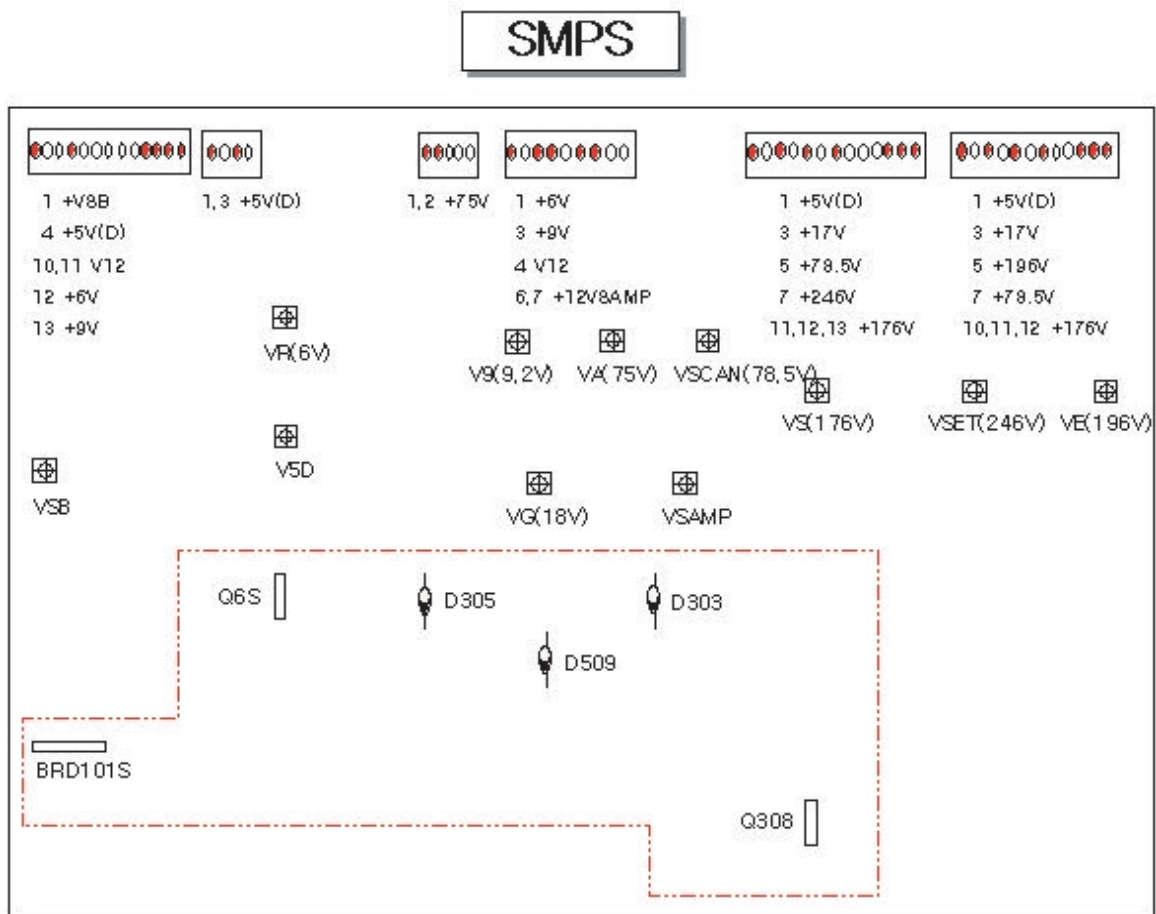
6-3-3 X Board

- Check that one of the output waveforms from X-OUT 1 or 2 is the same as that of the appendix 2 when power is supplied.



6-3-4 SMPS

- Check output voltage.
- If output voltage is not detected, check the following lists:
 - (1) Check fuse
 - (2) In case of +5V(D), check that D305 is short
 - (3) In case of VSAMP, check that D506 is short
 - (4) In case of VA, check that D303 is short
 - (5) In case of VS, check that pin 2 and 3 of Q303 are short
 - (6) In case of Q6S, check that pin 2 and 3 are short
 - (7) Check that BRD101S is short



6-3-5 Scaler Board

1. PW364 Input Clock

(1) MCKEXT

Check IC406(IC502) pin 5.

Power on : MCKEXT = 97.5MHz

Standby : MCKEXT = 48.75MHz

(2) MCKEXT, DCKEXT

Check IC407(ICS502) pin 25. DCKEXT = 65MHz

(3) VCLK

Check IC203(SDA9400) pin 26. VCLK = 27MHz

(4) GCLK

Check IC401(AD9884) pin 115(TP404).

GCLK is differently seen according to PC input signal format(VGA, SVGA, XGA)

GCLK = 15MHz ~ 50MHz(This value is apparently half of the clock frequency of the relevant PC input signal format.

2. VPC3230

- Check power is supplied(5V, 3.3V).
- Check Reset(pin 15) is high.
- Check I²C-bus(pins 13, 14)
- Check the signal input to Y signal(pin73), C signal(pin 71), PLL DVD-Y signal (pin 72).
- Check the output clocks LLC1(pin 28), LLC2(pin 27). (LLC1 = 13.5MHz, LLC2 = 27MHz)
- Check the output H sync(pin 56) and check V sync(pin 57) is output.
- Check output digital data.

3. SDA9400

- Check power is supplied(3.3V).
- Check Reset(pin 30) is high.
- Check I²C-bus(pins 20, 21)
- Check clock is input.(pins 28, 54 : 27MHz. pin 29 : 13.5MHz)
- Check digital data input.
- Check the input H sync (pin 23) = 15.75MHz, V sync (pin 22) = 60Hz
- Check digital data input.
- Check the output H sync (pin 60) = 31.5KHz, V sync (pin 61) = 60Hz, VCLK (pin 26) = 27MHz

4. AD9884(IC101)

- Check power is supplied(3.3V)
- Check I²C-bus(pins 29, 30)
- Check PC signal, HD-component signal is input.
- Check the input signal GREF (pin 40). The GREF signal applies to a fixed form of the input H sync signal.
- Check the output signal GFBK (pin 117). The GFBK signal applies to a fixed form of PLLD H sync signal.
- Check the output signal GCLK (pin 115). The GCLK is differently seen according to the PC input signal format(VGA, SVGA, XGA).
GCLK = 15MHz ~ 50MHz This value is apparently half of the clock frequency of the relevant PC input signal format.
- Check digital data output.

5. AD9884(IC801)

- Check power is supplied(3.3V).
- Check I²C-bus(pins 29, 30)
- Check Video signal is input.
- Check the input signal 2HS (pin 40 or TP406)
- Check the output signal VHS (pin 117 or TP409)
- Check the output signal VCLK (pin 115 or TP408)
- Check digital data input.

6. PW364 Reset

- When the Reset switch is pressed. if OTP01(29LV160T) pin 28(TP151) undergoes ransition. PW364 operates and OTP01 also does. Unless transition happens, it means PW364 is not operating.

7. PW364 Communication

- Operate the PC hyper terminal Settings are as follows :

Model Selection : Direct connect to com1

No. of Bit per second : 57600

Data Bit : 8

Parity : None

Stop Bit : 1

Flow Control : None

- Whenever the Reset switch is pressed, the following is displayed on the PC hyper terminal screen.

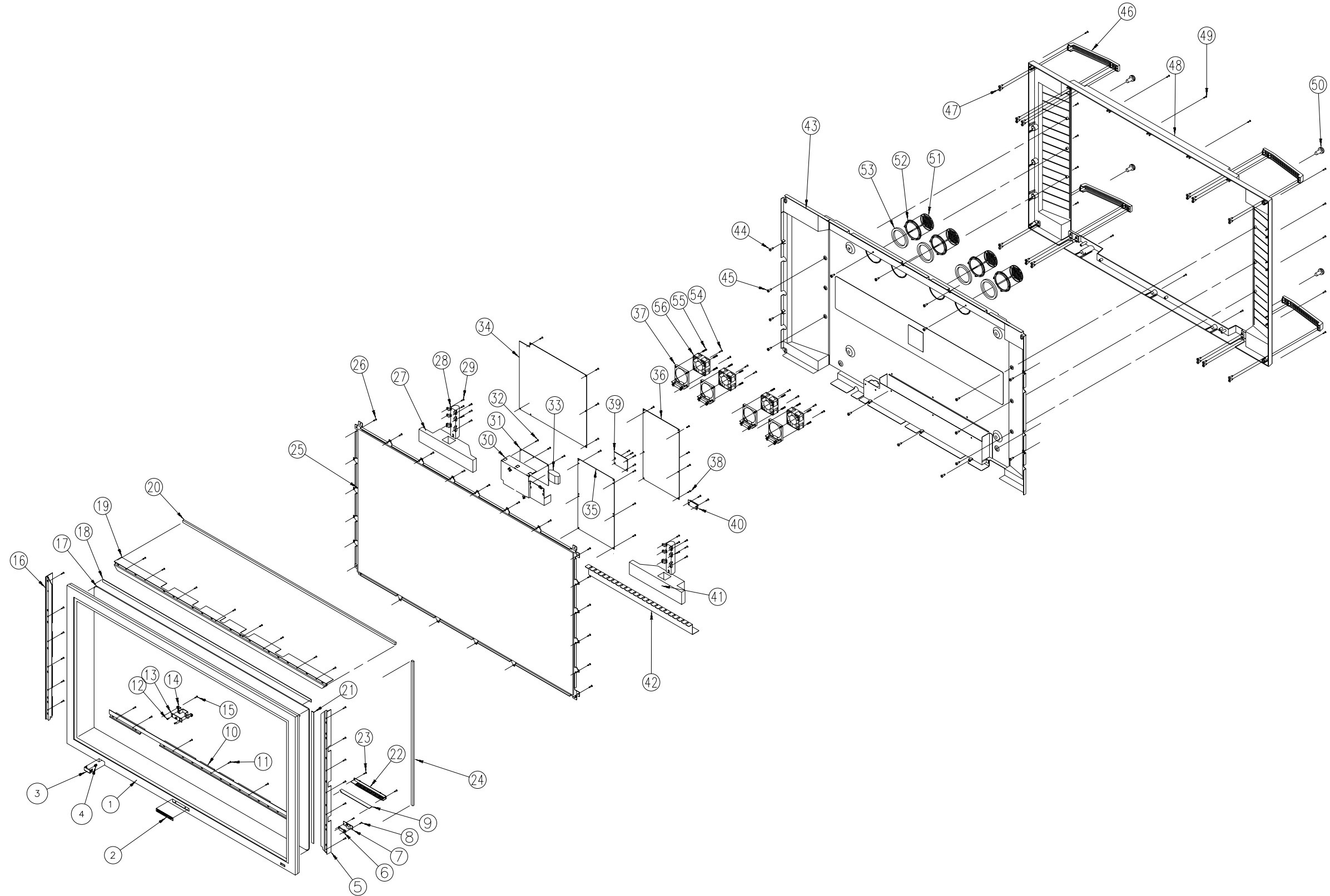
CBooter V1.5 & 2000.01.26

CBooter V1.5 & 2000.01.26

CBooter V1.5 & 2000.01.26

7. Exploded View & Parts List

7-1 PPM42S2X/XAA



NO	PART DESCRIPTION	CODE NO	SPEC.	Q'Ty	REMARK	NO	PART DESCRIPTION	CODE NO	SPEC.	Q'Ty	REMARK
1	CABINET-FRONT	AA64-01799F	42P2,HIPS VO,BLK,BK708P MONITOR MIJU	1		32	SCREW-ASS'Y MACH	6006-001035	WSP,PH,+,M3,L8,ZPC(YEL),SM10C	6	
2	BADGE-BEAND	AA64-01560B	PDP,AL FORGING,L68(45),SILVER,BK708PSS	1		33	FILTER-EMI AC LINE	2901-001222	250V,10A,UL,CSA,D,N,S,FI, ,22000PF, 24X50X62.3MIM,BK,HARNESS	1	
3	KNOB-MASTER	AA64-01566B	PDP,ABS,HB,BLK,BK708P NOSILK	1		34	ASSY-PBA, SMPS	AA98-00188A	,SPD-42P2A,D51A,42SD,90~264V, 47/63HZ,SEM	1	
4	SPRING-CS	AA61-60003J	-,SUS304,-,-,0D6,N7,0D6,-,-,-,-	1		35	ASSY PDP P-PBA,L-MAIN	BN96-00074A	,S422SD,D51A,D53A,42INCH,1F2A, SDI CODE LJ92-00573A	1	
5	BRACKET-FILTER SIDE L,ASSY	AA61-00171A	14F2A,HIPS,-,-,-,NTR,HB	1		36	ASSY-PCB MISC-SCALER	BN94-00290A	PPM42S2X,D53A	1	
6	WINDOW-RMC	AA64-01549B	PDP,ACRYL VIOLET,20:1	1		37	BRACKET-FAN,BASE	AA61-00579C	,SECC,T1.6	4	
7	ASSY SYB-PCB, REMOCON	AA95-01837F	SPD-42P2S,D51A,AA95-01560A	1		38	SCREW-ASS'Y MACH	6006-001035	WSP,PH,+,M3,L8,ZPC(YEL),SM10C	6	
8	SCREW-TAPTITE	6003-000333	RH,+,2S,M3,L10,ZPC(YEL)SWRCH1	2		39	ASSY PCB MISC-SOUND	BN94-00291A	PPM42S2X,D53A	1	
9	ASSY SUB-PCB CONTROL	AA95-01751D	PS42P2S,D53A,AA95*01582A	1		40	ASSY SUB TERMINAL	AA95-01770A	PS42P2S,D53A,AA95-01632A	1	
10	BRACKET-FILTER COT, ASSY	AA61-01062A	AL 6063 EXT,42P2,T1.2	1		41	SPONGE-EMI,BOT(L)	BN72-00316A	PDP,SHELD FROM	1	
11	SCREW-TAPTITE	6003-001020	RH,+,MB,M4,L10,ZPC(YEL)SWRCH10A,FP,-	28		42	COVER-TERMINAL	AA63-00491D	42P2,SUS,T0.3,MIJU(MONITOR)	1	
12	SCREW-ASS'Y MACH	6001-000578	TH,+,M3,L8,ZPC(YEL),SWRCH10A,FP,-	2		43	COVER-BACK, ASSY	BN63-00198A	42P2S,AL FAN,CMB,T1.2,SEA	1	
13	ASSY CUB-PCB, POWER ON/OFF	AA95-01833D	SPD-42P2S,D51A,AA95-01561A	1		44	SCREW-TAPTITE	6003-001019	RH,+,B,M4,L12,ZPC(BLK),SWRCH18	13	
14	BRACKET-POWER	AA61-00716B	,SECC,T1.0	1		45	SCREW-TAPTITE	6003-001020	RH,+,B,M4,L10,ZPC(YEL),SWRCH18	6	
15	SCREW-TAPTITE	6003-001026	RH,+,B,M4,L15,ZPC(YBLK),SWRCH18	2		46	HANDLE-SET	AA64-01551B	PDP,ABS,HB,BLK	4	
16	BRACKET-FILTER SIDE R, ASSY	AA61-00170A	53J2,-,-,-,-,HB,61-00079E(SIDE)	1		47	SCREW-TAPTITE	6003-001026	RH,+,B,M4,L15,ZPC(BLK),SWRCH18	24	
17	MIRROR-GLASS	AA67-00112A	42PDP,MESH,984*584,56%,T3.0,VS =922.2*518.4,0.15OHM	1		48	CABINET BACK	AA64-01802C	42P2,HIPS VO,BLK,WP1000	1	
18	SPONGE-EMI,FILTER	AA72-00018A	42P2,AHIELD-FORM,T1.2,D10,L560	2		49	SCREW-TAPPING	AA60-10050T	-,SWRCH18A,M4,L20MRH,+,2S,-,ZPC(BLK),-	16	
19	BRACKET-FILTER TOP,ASSY	AA61-01059A	AL,42P2,T1.2	1		50	SCREW-ASS'Y MACH	6006-001112	WP,PH,+,M8,L16,ZPC(BLK),SWRCH18A	4	
20	SPACER-FILTER	AA60-00110D	42P2,P/U VO,L,BLK	2		51	COVER-FAN	AA63-00366B	SPD-50P2H,SPT,TO.5	4	
21	SPOGE-EMI,FILTER	AA72-00018A	42P2,SHIELD-FORM,T1.2,D10,L560	2		52	HOLDER-FAN	AA61-00597B	SPD-50P2H,ABS VO,BLK	4	
22	KNOB-MASTER	AA64-01566B	PDP,ABS,HB,BLK,BK708P NO SILK	1		53	SPACER-FAN	AA60-00109A	SPD-50P2H,P/UFORM VO,BLK	4	
23	SCREW-TAPTITE	6003-001026	RH,+,B,M4,L15,ZPC(BLK),SWRCH18	2		54	SCREW-ASS'Y MACH	6006-001035	WSP,PH,+,M3,L8,ZPC(YEL),SM10C	8	
24	SPACER-FILTER	AA60-00110D	42P2,P/U VO,L,BLK	2		55	SCREW-ASS'Y MACH	6006-001017	WSP,PH,+,M4,L35,ZPC(YEL),SM10C	16	
25	ASSY-PANEL,PDP, SVC	AA98-00200A	,SPD-42P2S,D51A, 300X350X430XDP42SD04A	1		56	FAN-DC	3103-001109	12V,110MA,200RPM,0.34M^3/MI,-	4	
26	SCREW-TAPTITE	6003-001026	RH,+,B,M4,L15,ZPC(BLK),SWRCH18	26							
27	SPONGE-EMI,BOT(R)	BN72-00315A	PDP,SHELD FROM	1							
28	GUIDE-STAND	AA61-00584B	SPD-50P2H,AL,DIECASTING	2							
29	SCREW-ASS'Y MACH	6003-001039	WSP,PH,+,M4,L12,ZPC(YEL),SM10C	12							
30	BRACKET-LINE,FILTER	AA61-00582C	SPD-42P2H,SPC,T1.0,NI	1							
31	ASSY PCB POWER	AA94-07568A	SPD-42P2S,D51A,DOM	1							

8. Electrical Parts List

8-1 PARTS LIST FOR SERVICE

NO	Description	CODE NO.	Specification
1	ASSY PDP P-MODULE	BN96-00078A	M3, IF2A, 42P2S, D51A, S1.0, 1019, 2X616X56MM, SD, NTSC, 42INCH, DEPTH 89MM
2	ASSY-PANEL, PDP, SVC	AA98-00200A	, SPD-42P2S, D51A, 300X350X430, DP42SD04A
3	ASSY-PBA, X-MAIN	AA98-00206A	, 42SD, D51A, LJ41-00782A, SD42-XM-1.0, SDI, S1.0
4	ASSY-PBA, Y-MAIN	AA98-00209A	, 42SD, D51A, LJ41-00781A, SD42-YM-1.0, SDI, S1.0
5	ASSY PDP PBA, L-MAIN	BN96-00074A	, S42SD, D51A, D53A, 42INCH, IF2A, SDI CODE LJ92-000573A
6	ASSY-PBA, BUFF(UP)	AA98-00213A	, 42SD, D51A, LJ41-00783A, SD42-YK-1.0, SDI, S1.0
7	ASSY-PBA, BUFF(DOWN)	AA98-00215A	, 42SD, D51A, LJ41-00783B, SD42-YL-1.0, SDI, S1.0
8	ASSY-PBA, L-BUFF(E)	AA98-00218A	, 42SD, D51A, LJ41-00779A, SD42-LE-1.0, SDI, S1.0
9	ASSY-PBA, L-BUFF(F)	AA98-00221A	, 42SD, D51A, LJ41-00780A, SD42-LF-1.0, SDI, S1.0
10	FAN	AA31-00003B	TA225DC(M33394), PLASTIC, BRACKRT: AA61-00579C
11	ASSY-PBA, SMPS	AA98-00188A	SPD-42P2S, D51A, 42SD, 90+~264V, 47/63HZ, SEM
12	ASSY PCB MISC-SCALER	BN94-00290A	PPM42S2X, D53A
13	ASSY-PBA, AC-FILTER	AA94-07568A	SPD-42P2S, D51A, DOM
14	ASSY SUB-PCB, REMOCON	AA95-01837F	SPD-42P2S, D51A, AA95-001560A
15	ASSY SUB-PCB, POWER ON/OFF	AA95-01833D	SPD-42P2S, D51A, AA95-01561A
16	ASSY SUB-PCB, TERMINAL	AA95-01770A	PS42P2S, D53A, AA95-01632A
17	ASSY SUB-PCB, CONTROL	AA95-01751D	PS42P2S, D53A, AA95-01582A
18	ASSY PCB MISC-SOUND	BN94-00291A	PPM42S2X, D53A
19	REMOCON	AA59-00222A	, TM63, PDP, PW364, 44, SPK4215M
20	POWER-CORD	AA39-10004E	, -KJIP120/KJIC303, SVT 3/18AWG, 1.
21	MIRROR-GLASS	AA67-00112A	42INCH, PIS, MESH, 55% 1.15OHM
22	MANUAL USERS	BN68-00258A	PPM42S2, ENG, S/W120G, D53A, A4
23	RS232C CABLE	AA39-00311A	PDP, 9P/IP, UL2851 # 28, 5000MM, UL2851, BLK, DSUB/STEREO PLUG, 2C, SJ01-01-296
24	S/W DRIVER	AA59-00261A	PPM42S2, INSTALL-S/W, BASIC, CD-ROM

Level	Loc. No.	Code No.	Description ; Specification	Remark
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ASSY COVER REAR

1	*	BN90-00278E	ASSY COVER REAR;42P2,PPM42S2X/XAA,M,MIJU	S.N.A
..2		BN91-00334A	ASSY CABINET BACK;,HIPS V0 BLK,WP1000,42	
...3	COB+CB	6003-001019	SCREW-TAPTITE;RH,+,B,M4,L12,ZPC(BLK),SWR	S.N.A
...3	COB+CB	6003-001020	SCREW-TAPTITE;RH,+,B,M4,L10,ZPC(YEL),SWR	S.N.A
...3	COB+HS	6003-001026	SCREW-TAPTITE;RH,+,B,M4,L15,ZPC(BLK),SWR	S.N.A
...3		AA64-01551B	HANDLE-SET;PDP,ABS,HB,BLK	S.N.A
...3		AA64-01802C	CABINET BACK;42P2,HIPS V0,BLK,WP1000	
...3		AA65-00003A	CABLE-CLAMP;SIR-T100,PE BLACK,-,-,-	S.N.A
...3		BN63-00198A	COVER-BACK,ASSY;42P2S,AL FAN,VMB,T1.2,SE	
...4		AA63-00433A	COVER-BACK,BOT;42P2,AL,T1.2	S.N.A
...4		BN63-00197A	COVER-BACK;42P2S,AL FAN,VMB,T1.2,MIJU(MO	
...3		AA63-00366B	COVER-FAN;SPD-50P2H,SPT,TO.5	
...3		AA61-00597B	HOLDER-FAN;SPD-50P2H,ABS V0,BLK	S.N.A
...3		AA60-00109A	SPACER-FAN;SPD-50P2H,P/UFORM V0,BLK	

ASSY P/MATERIAL

1	*	AA92-03150A	ASSY P/MATERIAL;PS42P2SDX/XEC	S.N.A
..2		AA61-20285A	HOLDER-BOX;3456,PP,-,-,-,WHT,VO	S.N.A
..2		AA60-40006A	PIN-STAPLE;-,-,H18,33X17.8X2.4,-,-,AUTO	S.N.A

ASSY LABEL

1	*	BN92-00386E	ASSY LABEL;PPM42S2X/XAA,PPM42S2	
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Level	Loc. No.	Code No.	Description ; Specification	Remark
-------	----------	----------	-----------------------------	--------

ASSY BOX

1	*	BN92-00373G	ASSY BOX;42P2S,PPM42S2X/XAA	
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ASSY ACCESSORY

1	*	BN92-00415F	ASSY ACCESSORY;PPM42S2X/XAA,PPM42S2,ENG	
..2		BN68-00258A	MANUAL USERS;PPM42S2,ENG,S/W120G,D53A,A4	
..2		AA59-00261A	S/W DRIVER;PPM42S2 ,INSTALL-S/W,BASIC,CD	
..2		AA39-10004E	POWER-CORD;- ,KJP120/KJC303,SVT 3/18AWG,1	
..2		4301-000103	BATTERY-ALKALINE;1.5V,750mAH,AAA,10.5x44	S.N.A
..2		AA39-00288A	CBF SIGNAL;HPL5025M,15P/15P,2990,1830MM,	
..2		AA39-00311A	CBF SIGNAL;PDP,9P/1P,UL2851#28,5000MM,UL	
..2		AA39-40001E	CABLE-S.VHS;;,1500MM	
..2		AA59-00222A	REMOCON;;,TM63,PDP,PW364,44,SPK4215M	
...3		2802-000194	RESONATOR-CERAMIC;8MHz,1.0%,TP,8.5x4.5x5	
...3		AA09-00275A	IC MICOM;Z86L8808SSC-R51PX,SOP,ST,SZTM-8	

MEMO

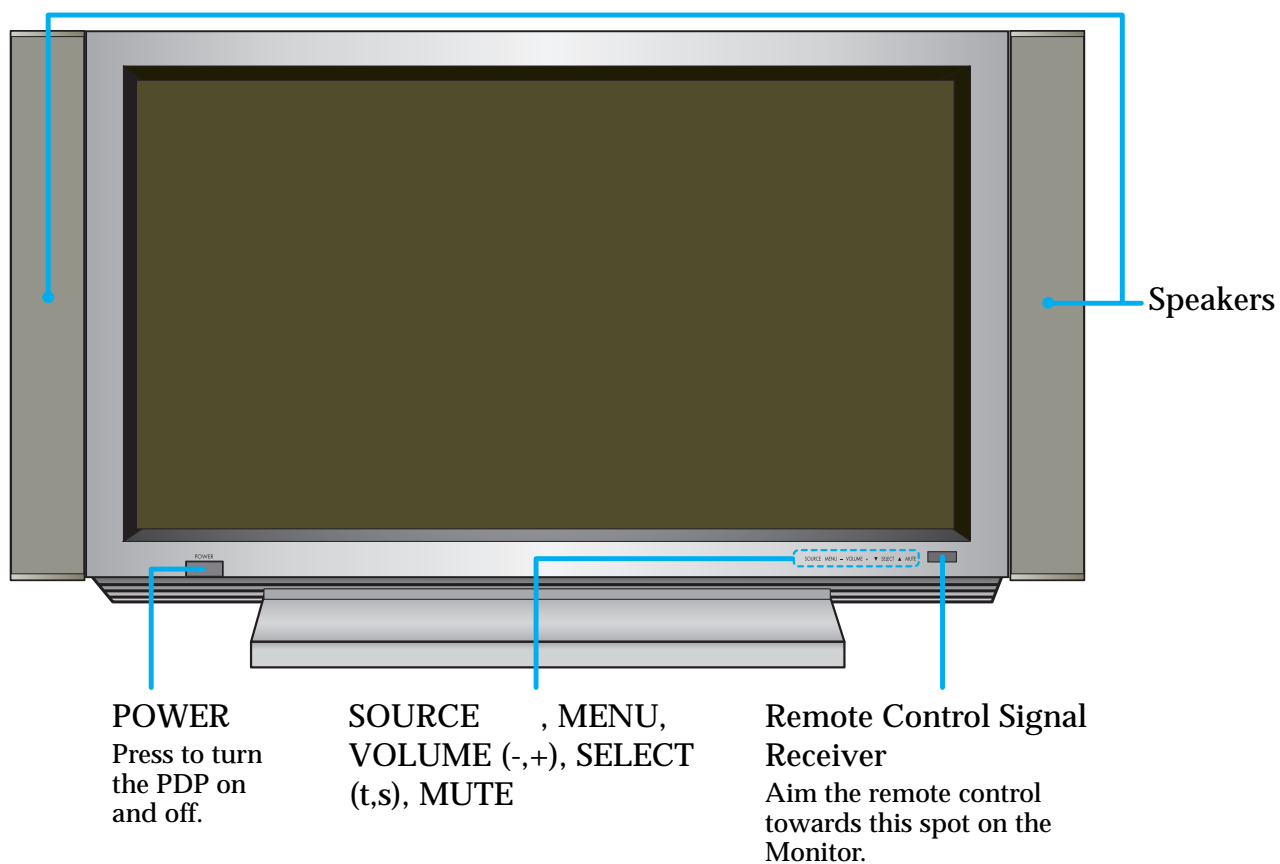
9. Handling Description

9-1 Basic Description

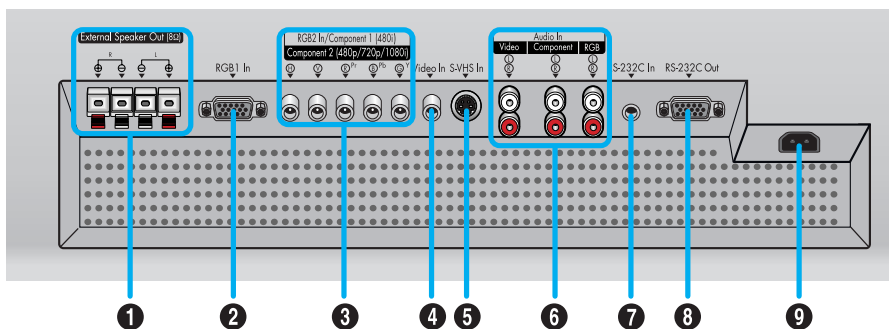
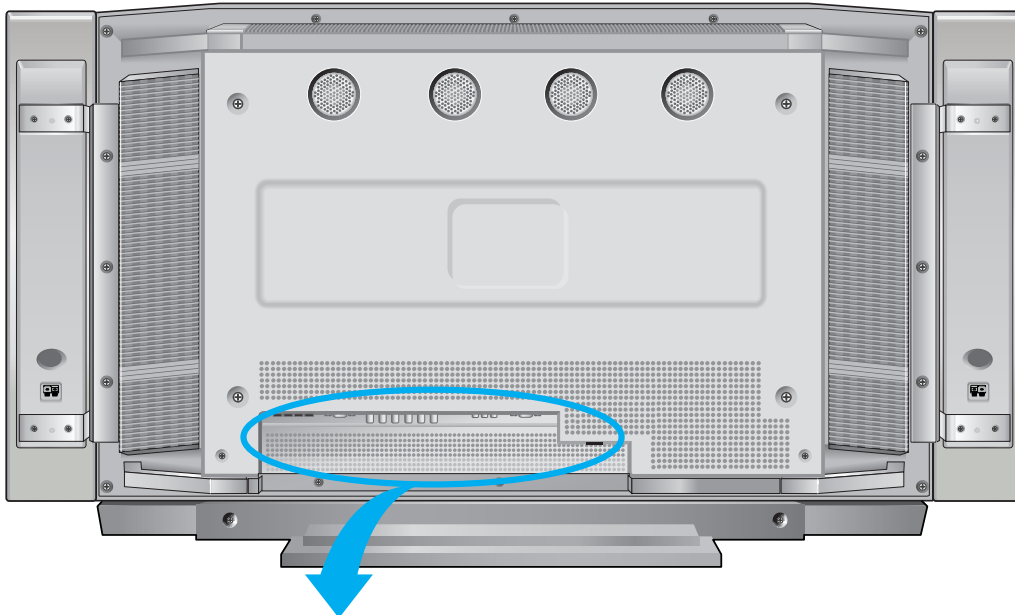
9-1-1 The Name of Each Part

9-1-1(A) PDP(Plasma Display Panel)

Front Panel



Rear Panel



1 External Speaker Out jacks

Connect external speakers.

2 RGB Input 1 jack (15pin)

Connect to the video output jack on your PC.

3 RGB Input 2/Component Video

Input jacks (H/V/R/B/G, Y/P_b/P_r)

RGB input2/Component video input jacks are BNC connectors.

4 Video Input jack

Connect a video signal from external sources such as VCRs or DVD players.

5 S-VHS Input jack

Connect a S-Video signal from an S-VHS VCR or DVD player.

6 Audio Input

(Video/Component/RGB) jacks

Connect a audio signal from external sources such as VCRs, PC or DVD players.

7 RS-232C Input jack

Connect the RS-232C input jack to your PC.

8 RS-232C Output jack

Connect the RS-232C output jack to another PDP.

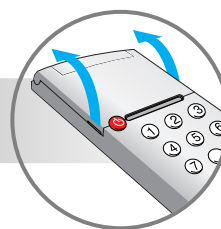
9 Power Input jack

Connect the supplied power cord.

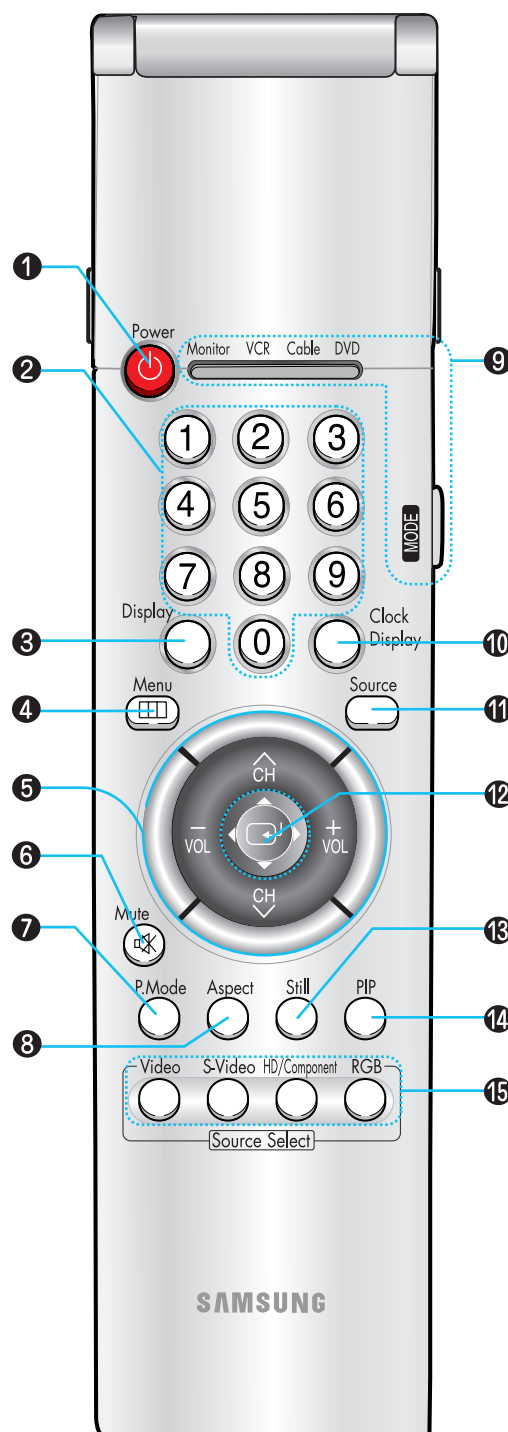
9-1-1(B) REMOTE CONTROL

Remote Control

Flip the cover open
in the arrow direction.



- 1 Power button**
Turns the PDP on and off.
- 2 Number buttons**
- 3 Display button**
Press to display information on the PDP screen.
- 4 Menu button**
Displays the main on-screen menu.
- 5 CH (Channel) and VOL (Volume) buttons**
Channel buttons : Not available for this Monitor.
Volume buttons : Press to control the Volume.
- 6 Mute button**
Press to mute the PDP sound.
- 7 P.Mode button**
Adjust the PDP picture by selecting one of the preset factory settings (or select your personal, customized picture settings.)
- 8 Aspect button (Not available in PC Mode)**
Press to change the screen size.
- 9 Mode button**
Selects a target device to be controlled by the Samsung remote control (ie., VCR, Cable, or DVD players).
- 10 Clock Display button**
Press to display clock on the PDP screen.
- 11 Source button**
Press to display all of the available video sources (ie., Video, S-Video, Component1, Component2, RGB1, RGB2).
- 12 Joystick button**
Use to highlight on-screen menu items and change menu values.
- 13 Still button**
Press to pause the current screen.
- 14 PIP button**
Activates picture in picture.
- 15 Source selection buttons**
Press to directly select Video, S-Video, Component1, Component2 or RGB1, RGB2.



16 VCR control buttons

Controls VCR tape functions: Stop, Rewind, Play/Pause, Fast Forward.

17 Set button

Used during set up of this remote control, so that it will work compatibly with other devices (VCR, cable box, DVD, etc.)

18 Clock set button

Press to set clock.

19 PIP control buttons

Source : Press to select one of the available signal sources for the PIP window.

Swap : In Video and S-Video mode, press to exchange to video signal that is currently displayed on the main screen with the signal in the PIP window.

Size : Press to make the PIP window larger or smaller.

Locate : Press to move the PIP window to any on the four corners of the screen.

20 PC control buttons

Auto Adjust
Scaling
Zoom

21 Sleep button

Press to select a preset time interval for automatic shutoff.

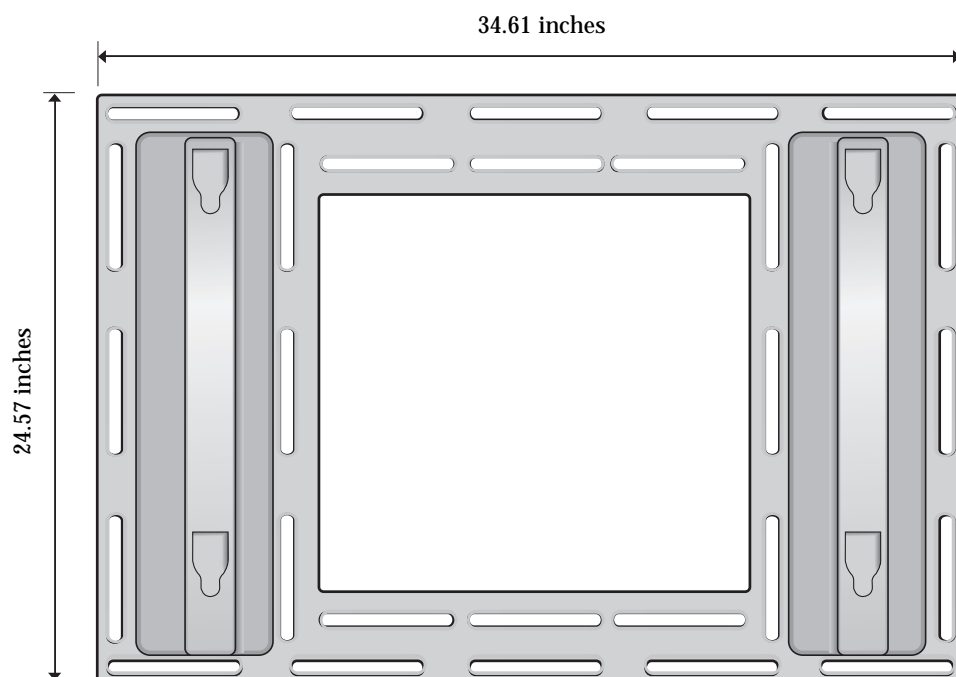


9-2 Wall Mount

9-2-1 Notice for installing

1. Do not install the PDP in any location other than vertical walls.
2. To protect the performance of the PDP and prevent problems, avoid the following places.
 - 1 Do not install next to smoke and fire detectors.
 - 1 Do not install in an area subjected to vibration.
 - 1 Do not install in an area subjected to high voltage.
 - 1 Do not install near or around any heating apparatus.
3. Use only recommended parts and components

9-2-2 Parts (Wall attachment panel is sold separately. Check with your dealer or Samsung)



bolt

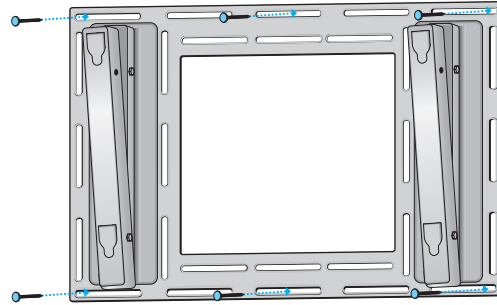


Insulation holder

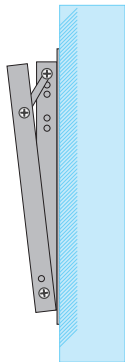
9-2-3 Installing the Display on the Wall Attachment Panel :

1. See the drawing of the wall attachment panel shown in page 14 to check for the stability of the wall where the PDP is to be installed. If the wall is not strong enough to support the PDP, strengthen the wall before installation.

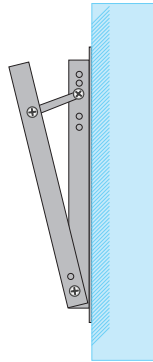
2. Fix the wall attachment panel on the wall using bolts as shown in the following figure: Fixing bolts must protrude from the wall approx. 0.6 inches



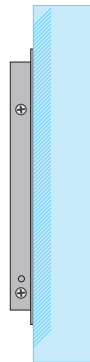
3. Using the wall attachment panel, you may adjust the angle of the display from 0 to 20 degrees. The angle can be set in 5 stages with 5 degrees of distance each, using the angle control holes on the sides of the pane.



When the angle has been set to 5 degrees.

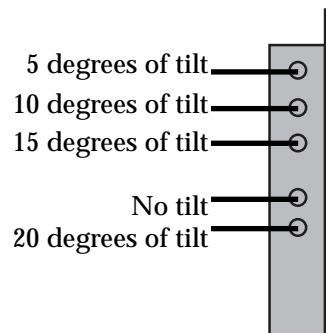


When the angle has been set to 15 degrees.



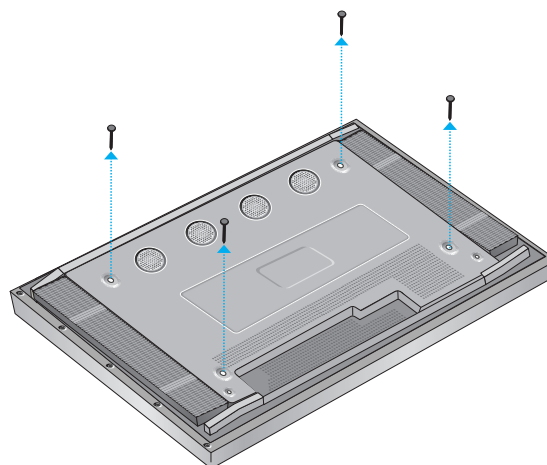
When the panel hasn't been tilted.

Angle control holes



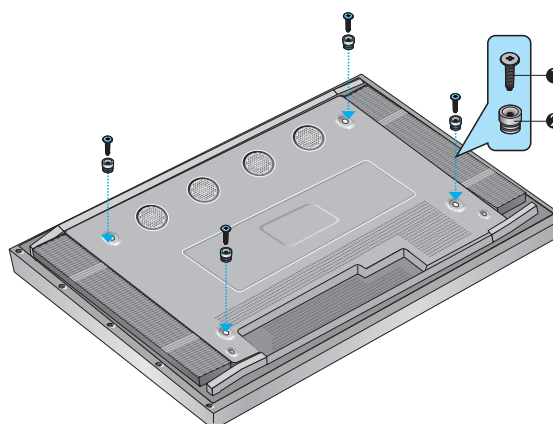
Continued...

- Remove four large screws from the rear side of the display.

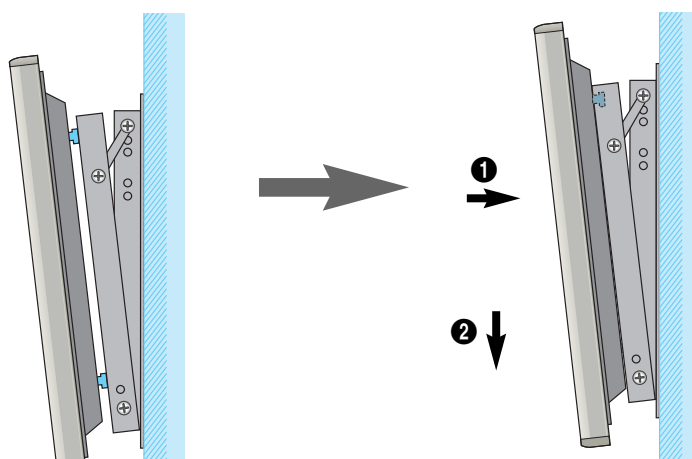


- Insert the bolts and insulations into the four screwholes as shown in the following figure:

- ① Bolt
- ② Insulation holder



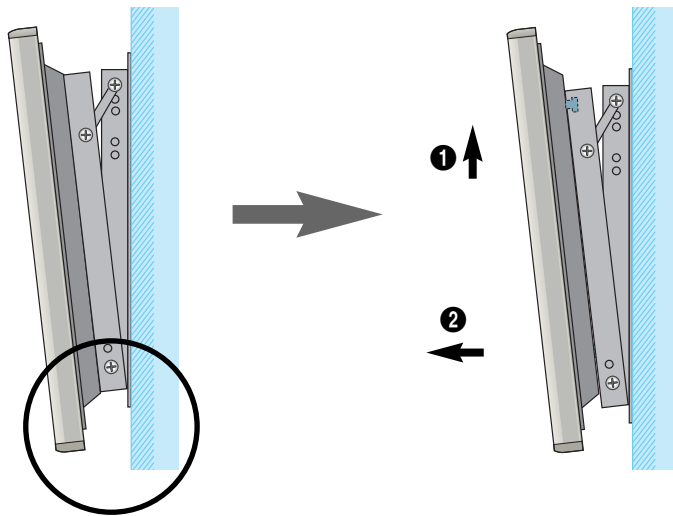
- Put the insulation rubber point protruding from the rear top of the display in the groove on the top of the wall attachment panel. Lift up the display a little bit so that the insulation rubber point at the bottom of the rear side of the display is put in the groove at the bottom of the wall attachment panel. (Do not lift the display with any pressure. The insulation rubber at the top may be taken off.)



9-2-4 Separating the Display from the Wall Attachment Panel :

Remove the fixing bolts from both sides (left and right) of the wall attachment panel. Lift and pull the bottom of the display a small amount, to separate the insulation holder point from the bottom of the wall attachment panel.

Lift the display and separate the insulation holder point from the groove on top of the wall attachment panel.



10. Glossary

AC PDP :

Plasma display driven by alternating current plasma electric discharge.

Address discharge(Reference : scan and data) :

Term with two meanings that can be used for both scan and data (write or erase) discharge.

Address Electrode(Reference : scan and data electrode) :

Term with two meanings that can be used for both scan and data electrodes.

Address pulse(Reference : scan and data pulse) :

Address drive wave form

Address voltage(reference; scan and data voltage) :

Address drive amplitude of vibration

Addressing :

Process that gives authorization to cells to allow for turning on and off by drive wave form.

Addressing speed :

Time necessary for writing and erasing.

ADS, address display separation :

Drive tech that separates address pulse temporarily from sustained voltage.

Aging :

The change of operation expectancy- for example, operation voltage change and luminance decline-related characteristics.

Angular distribution :

Characteristics which change as function of angles between perpendicularity and surface. referring to dependency on angles of, for example, luminance or chromaticity.

Aperture ratio :

Referring to the ratio of an element activation area to the gross area.

Area luminance :

Luminance measured in relatively large area.

Aspect ratio :

The ratio of screen width to height.

Auto power control :

Circuit means for controlling panel's average or maximum power.

Auxillary anode :

Anode where discharge of DC panel has little contribution to light output power.

Back ground luminance :

Referring to the panel luminance in off mode or black screen, in other words, luminance in the vicinity of the screen.

Barrier rib :

barriers that cross all the gaps of wafers dividing the cells in panel.

Black stripe :

black substance located in between the fluorescent areas to bring about improvement in contrast by reflection ratio decline. Generally, this is striped.

Bright defect :

defects that occur when the image is rather bright than accurate.

Brightness(Reference : luminance) :

visible and subjective quality, for example, how bright matters look or how much visible rays are perceived.

Notice) Do not get confused luminance with brightness because those two are not the same. Brightness is subjective while luminance is objective.

Brun in :

element's initial operation section that takes place until the element stabilizes or the initial expectancy expiration is detected.

Bus electrode :

aggregate of sustained electrodes that are bussed together.

Cathode electrode :

cathode electrified electrode that releases electrode from element. In AC plasma panel, polarity switches in every half a cycle.

Cell :

capacity corresponding to each electric discharge. In general, it is defined by the shape of substrates and electrodes but can be defined by partitions.

Cell gap :

measurements identifying the gaps between substrates.

Cell pitch :

measurement that identifies the cells from the surface of substrates. It varies depending on the direction of rows and columns.

Charge transfer curves :

curves expressing the quantity of electric charge that is transferred, as the function of drive wave form characteristics.(for example, voltage, time and others)

Color arrangement(in other words, sub-pixel arrangement) :

term expressing the location of one pixel consisted of sub color pixels.

Color coordinates, CIE 1931 :

Color image expressing method in color dimension, originated from CIE standard of 1931, expressed by X, Y and Z. Among those three, Y element corresponds to luminous flux that is expressed as lumen while X and Y are values that express red and purple element of luminous flux. Colors of matter are expressed as color coordinates pair (x, y). Here $x=X/(X+Y+Z)$, $y=Y/(X+Y+Z)$.

Method for colors, known as (u, v), where image colors are expressed in more even color dimension.

Colors of matter are expressed as color coordinates pair (u, v). Here, $u=4X/(X+15Y+3Z)$, $y=6Y/(X+15Y+3Z)$.

Color coordinates, CIE 1960 :

Method for colors, known as (u, v), where image colors are expressed in more even color dimension. colors of matter are expressed as color coordinates pair(u, v). Here, $u=4X/(X+15Y+3Z)$, $v=6Y/(X+15Y+3Z)$.

Color coordinates, CIE 1976

Method for colors, known as (u', v'), where revised image colors are expressed in more even color dimension. v' is 1.5-fold of recommended v value of 1960. The color of matter is expressed as color coordinates pair (u', v'). Here, $u'=4X/(X+15Y+3Z)$, $v'= 9Y/(X+15Y+3Z)$.

Color coordinates, CIE 1976 CIELUV and CIELAB :

Three dimensional parameters expressing with u' and v' including Ω_{∞}^{\oplus} against chromaticity and luminance of standard white light in display. Among the parameters, only CIELUV gets to have proper color space where additional two blend light appears in line segment. (refer to CIE Publication 15.2, Colorimetry 1st edition 1976, 2nd edition 1986)

Color depth :

The number of digital bit allocated to each major color.

Color gamut :

Physically realizable color space area.

Color reproducibility (Refer to color gamut) :

The expression of realizable colors limited by color information distinction or fluorescent substance chromaticity.

Color temperature, correlated (symbol CCT) :

Seemingly temperature expressed with absolute temperature of black body radiation with the closest chromaticity. This can be expressed as CCT, in the form of C. S. McCamy. $CCT=437N^3+3601n^2+5517$, $n=(x-0.3320)/(0.1858-y)$ and x, y =color coordinates of CIE 1931.

Columm electrode :

Vertically successive electrodes. It generally refers to data electrodes. When panel is installed along the photograph, this can be arranged along the horizontal direction.

Concurrent driving method :

Driving method to disperse address pulse and scan pulse at equal distance.

Contrast ratio Columm electrode :

Ratio of white luminance to black luminance of image. This measurement has many parameters, so measurers are required to explain the consideration for measurement to make understood the meaning of the measurement. The parameters of contrast ratio are as follows.

- n CA - ratio of center luminance in all white screen to center luminance of all black screen on the condition of light being spreading around.
- n CG - ratio of white luminance to black luminance in successive arrangement of white and black lines at equal distance.
- n CL - ratio of white luminance to black luminance in white line against black screen of black line against white screen.
- n CR - the ratio of white luminance to black luminance.

- n Cm - Michelson contrast or contrast modulation:
Here, L_w is the luminance of the color white while L_b is the luminance of the color black.
- n CT - Threshold contrast ratio: the minimum contrast ratio that is permissive, in general.

Chip on board(COB) :

PCB with IC on substrate.

Dark defect :

Defects in the brighter image realization than normal one.

Data electrode :

Electrodes allowed for controlling electric discharge by changing the cell's state to switch on from off (and vice versa) in AC plasma panel.

Data electrode driver :

Driving circuit to be attached to data electrode.

Data write pulse :

Wave form for data electrode that switches from off to on.

Data erase pulse :

Wave form for data electrode that switches from on to off.

DC PDP :

Display panel whose plasma discharge is driven by direct current.

Decay time :

Time required for parameters to drop from certain level to another. It can be time necessary for dropping from 90% to 10%, or to e-1 level of the initial value, or to certain irreversibility.

Dielectric layer :

Dielectric layer with larger sustained electric constant.

Discharge :

1. neutralization of electric charge (for example, voltage decrease of capacitor)
2. electric current flow in dielectric media such as gas.

Discharge current :

Discharge electric current.

Discharge electrode :

Another term for sustained electrode.

Discharge efficiency :

Another term for gloss efficiency

Discharge gap :

The gap among sustained electrodes in discharge space of three-electrode plasma panel.

Discharge slit :

(Refer to discharge gap)

Displacement current :

Electric current flow through capacitor that includes atomic rearrangement of discharge within electric matter.

Display color number (color number possible to be displayed with other words.) :
displayable individual color's number.

Display Diagonal :

Diagonal size of display contour

Display efficiency :

The ratio of gloss output divided by the entire display power.

Display height :

Height of display contour

Display scan electrode :

(Refer to scan electrode)

Display width :

Width of display contour

Displayed color :

Refer to displayed color number.

Displayed color number :

Color numbers that can be made by display.

Dot (Refer to cell, pixel and subpixel) :

The term is hard to be defined because it is not clear if the term refers to full color pixel or subpixel. The term is used when referring to color related elements that make up full color pixel or subpixel.

Dot pitch :

(Ambiguous expression. Refer to dot, cell pitch, pixel pitch and subpixel pitch.)

Driving waveform :

Expressing $\propto \sqrt{\Omega}$ change of driving signal voltage.

Driving scheme :

Expressing the thought applying driving voltage to display.

Efficacy :

Refer to luminous efficacy.

Energy recovery circuit :

Circuit degauss caught after reusing the power that drove AC plasma panel.

Erase :

Process where cells are erased from AC plasma panel.

Erase pulse :

Cell erasing waveform

Erase voltage :

Erase pulse voltage required for erasing cells from AC plasma panel.[symbol : V_e]

Evacuating (Interchangeable terms : evacuation, exhaust) :

Process where unwanted gas is rid from device.

Exhaust tubulation (Interchangeable terms: exhaust tube, exhaust pipe) :

Tube shaped hole in device connected to external vacuum pump, for controlling the initiation from device during process. This is usually glass tube that prevents with flannelet after filling proper gas

Filling gas (Refer to gas mixture) :

After removing air, plasma panel goes through filling with proper electric and optical gas. Therefore, panel gas composition is commonly called "filling gas".

Firing voltage :

Minimum voltage where triggers discharge in plasma device[symbol : V_f]

Flicker :

Fast and instant changes in luminance, perceivable in almost regular luminance experiment pattern.

Front substrate :

Substrates closer to the viewers, made of transparent material such as glass

Full color display :

Full color image (for example, image with more than 8 bit color tone) realizable display

Fpc(Flexible Printed Curcuit) :

Flexible substrates with circuited copper foil on polyimide

Gas mixing ratio (Interchangeable terms: gas mixture, gas composition) :

Gas composition within plasma device. It is usually expressed with ratio of the constituent gas.

Gas voltage (Interchangeable terms: gas break down voltage) :

Voltage where electrode and ion within plasma device can generate additional electrodes and ions.
-Thus, increasing the electric current within the device sharply. (break down or overflowing)

Glass substrate :

Substrates consisted of glass

Glow discharge :

Plasma discharge taking place under pressure of tens of millimeter. This is defined by ionization generated by activated electrons in discharge space and electron release in cathode by ion bombardment.

Gradation :

Gradual change in characteristics such as luminance and chromaticity

Gray scale :

The range of luminance acquired when displayed from black to white.

High strain point glass :

Glass of which strain point (temperature with viscosity of 1014.5 poise) is relatively high

Image retention :

Continuous existence of image after the stimulation is removed.

Image sticking :

(Refer to Image retention.)

Interconnect pad groups :

A group of connection terminals that attach to individual connector. (also referred to as terminal block.)

Interconnect pad pitch :

Mutual measurements for individual of interconnect pad group.

Interconnect pad spacing :

The size of non-electric conductive area between individual terminal.

Inter-electrode gap :

In Three electrodes plasma panel, the measurement of sustained voltage separated from outside discharge space.

Ion bombardment :

The bombardment of energetic ions in the surface of solid matter. The transfer of kinetic energy toward surface from ions can cause electron release, ion or neutron release and temperature change in surface.

Life time :

Time during device exerts its function. Commonly known as mean time failure (MTTF).

Low melting point glass :

Glass of which melting point (temperature with viscosity of 1014.5 poise) is relatively low.

Since glass is non-crystalline, the word melting is not appropriate, but it gets more fluid as it becomes hot.

Luminance :

Colloquial term for measurement of brightness of display.

It also refers to display related CIE Y constituent. It is expressed by cd/m².

Luminance efficacy :

It refers to gloss output against the total display consumption power. It is calculated by the value generated through dividing gloss output of ∞¹ white substance with gross consumption power. It is expressed as lumen/watt.

Luminance efficiency :

Gloss output value according to consumption power increase, calculated by the value generated through dividing gloss output of ∞¹ white substance with white screen power consumption increase against black screen. It is expressed as lumen/watt.

Luminance loading :

Luminance decline that takes place when white square luminance increases into full size all white square.

Matrix(type) PDP :

Plasma display panel made up of matrix with rows and columns.

Matrix type :

Refer to matrix PDP

Maximum firing voltage :

Voltage value required for triggering discharge in all cells.

Maximum sustain voltage :

Maximum drive voltage required not to turn off the cells.

Memory margin :

The disparity between the maximum sustained voltage for keeping discharge and the sustained voltage for turning off the cells

Memory type PDP :

Refer to AC Plasma Panel that has memory. PDP made up of cells that keep turned on or off until switch occurs.

MgO layer :

In bombardment of electrons and ions, MgO's high electron release rate, like cathode application, makes it easier to release electrons.

MgO protecting layer (Refer MgO layer) :

MgO layer on fluorescent material has secondary benefit that prevents fluorescent degradation by ion bombardment.

Minimum firing voltage :

Minimum voltage that can turn on any cells.[symbol : V1]

Minimum sustain voltage :

Minimum sustain voltage that keeps turned on cell on.[symbol : Vsm1]

Monochrome display Minimum sustain voltage :

Display that only expresses a limited color such as white, green and amber.

Multi-color display :

Display that can express multiple colors .if not all colors.

Non-discharge slit :

(Refer to inter electrode gap)

Operating margin :

AC PDP voltage range that keeps cells turned on or off. Generally, its value gets less than memory margin because of additional factors such as temperature effect, gloss ionization effect and waveform change.

Operating window :

Actual voltage range that keeps cells turned on or off in any drive levels and surrounding environment.

Operating window degradation :

Gradual decline in operating window, according to operating time.

Opposed discharge :

Traditional two-electrode plasma panel structure where discharge occurs between the two sustained electrodes across from each other.

Opposed discharge PDP :

(Refer to opposed discharge.)

Peak luminance :

Maximum luminance generated in one pixel in panel.

Peak luminance enhancement :

Circuit and drive technology that accommodates increasing peak luminance.

Phosphor degradation :

Gradual decline in fluorescence efficiency according to operating expectancy.

Phosphor layer :

Thin layer made up of phosphor. Fluorescence substance must be thick enough to optimize transferring the ultraviolet rays from plasma discharge to visible light

Pixel, picture element :

The smallest unit that can display the entire range of luminance and chromaticity. Generally, pixel consists of sub pixels (or dots).

Pixel arrangement :

Expression of sub pixels within a pixel.

Pixel count :

The number of pixels that make up a display. It is described as the number of column pixels against the number of row pixels.

Pixel pitch :

The distance between the centers of the two closest pixels. Move as far as the pitch and reach the identical location.

Plasma display :

Electrically driven display device for causing electric discharge in gas within device. Electric energy generates light with atomic light release or from proper colored fluorescence substance.

Positive column discharge :

The plasma area for long glow discharge. This area is a low electric field but relatively electric conductive plasma area.

Pre discharge :

Cell's state where pre discharge is taking place. In this case, cell's state becomes electric conductive due to formation of discharge generated by ionization process of gas.

Priming :

The stage where ions are generated for forming discharge. Generally, this is required for injection.

Priming pulse :

Electric waveform to define the proper conditions for the next cell discharge. [symbol : Pp]

Priming voltage :

Voltage of priming pulse. [symbol : Vp]

Protecting layer :

The layers applied to the device function constituents (for example, fluorescence, electrode and glass layers).

Quantum efficiency :

Substrates farther from the viewers. These can be opaque.

Rear substrate :

Efficiency measurement that is directly expressed with the number of output particles against the number of input particles. In case of plasma panel, the number of photons in visible area, generated from photons in ultraviolet area

Reset :

(Refer to erase.)

Reset discharge, Reset pulse :

(Refer to erase.)

Resolution :

Display's ability to enable to distinguish the matters close to each other. It is confusing with addressibility that generates pattern undistinguishable to the eyes.

Row electrodes :

Horizontally successive electrodes. In terms of traditional drive concept, these are the sustained electrodes. If the panel is installed toward portrait, these row electrodes can be arranged horizontally.

Sand discharge :

Process where grinding of surface occurs. It is used for making three dimensional surface in lithography or silt in sheet.

Scan discharge :

Discharge injected along the pair of sustained electrodes.

Scan electrode :

Electrodes of the pair of sustained electrodes that inject discharge downward along the panel columns.

Scan pulse :

Waveform that injects discharge with new columns.
Optic defects where scratches display over certain size.

Seal :

Combining the substrates or substrate with ventilation tube.

Seal layer :

Material layer that provides the connection of substrates. This can be a single layer of solder glass (frit) or the combination of solder glass and ring.

Sealing :

Process where free electrons that get out of the surface by extracting static electricity field when energetic electrons or ions are limited to a surface.

Secondary electron emission :

Process where drags discharged cell to certain waveform. This could occur before ionization offset when cell voltage decreases.

Self erase :

Plasma display in the form where stimulating discharge occurs for discharge process precedes below panel.

Self-scan type PDP :

Plasma display in the form where stimulating discharge occurs for discharge process precedes below panel.

Self-shift type PDP :

Process of combining substrates. High temperature process that melts solder glass combining substrates.

Space charge :

Mutual repulsion caused by accumulation of electric charge of similar signal.

Stripe rib :

Stripe shaped partition structure. It follows panel column direction.

Sub frame :

(Refer to sub field)

Sub field :

A part of panel

Surface charge :

It refers to the location of discharge in AS plasma panel where sustained electrodes are on the same surface.

Surface charge PDP :

AS plasma panel where sustained electrodes are on the same surface.

Sustain :

Discharge in AC plasma panel that keeps on or off until the cell is erased or written. Sustained electrodes are divided into bus (common electrodes) and addressable electrodes.

Sustain driver :

Circuit that drives sustained electrodes.

Sustain electrode :

Electrodes driven by AC voltage that provides plasma with energy major parts. This electrode is driven by enough waveform to keep discharge of turned on state. In turned off cell, trigger discharge does not takes place.

Sustain margin :

The disparity between sustained voltage that keeps turned on cells and sustained voltage that can turn off cells.

Sustain pulse :

Sustained drive waveform[symbol : Ps]

Sustain voltage :

Voltage level of sustained waveform

Thermal compaction :

Substrates successive density increase observed by substrates pattern contraction.

Thermal radiation :

Radiation in infrared rays over 800nm.

Three electrode type :

Modern AC panel has three electrodes for each cell and a pair of thermal electrodes provide cells with AC power. Data electrodes in opposite substrates provide unique writing and erasing signals to each cell

Time modulation driving method (Other terms: time division multiplex method) :

Modulation method in proportion to certain time applied to stimulation with regular output. Output strength is changed according to input time.

Tip pipe :

(Refer to exhaust turbulation.)

Townsend discharge :

Self sustained plasma discharge expressed by Townsend in 1901. This discharge requires 200v voltage.

Transparent electrode :

Electrode made up of transparent electric conductive matter such as ITO.

Two electrode type :

Original AC plasma panel used two electrodes that provide not only sustained waveform but also write and erase waveform.

Ultraviolet ray :

Ultraviolet light below 380nm in spectrum.

Vacuum ultraviolet :

Ultraviolet ray of wavelength below 200nm.

Viewing angle :

Vertical angle that can display the image. It is normally limited by the change in luminance and chromaticity.

Viewable screen diagonal :

Releasable screen diagonal length measured between outmost pixel edges

Viewrabel screen height :

Releasable screen height measured between outmost pixel edges

Viewrable screen width :

Releasable screen width measured between outmost pixel edges.

Visible defect :

Imperfection that prevents displaying with proper image.

Wall charge :

Pure accumulation of positive and negative charges in cell wall.

Wall charge erase pulse :

Pulse that neutralizes wall charge

Wall charge transfer curve :

Curve related to wall charge pulse parameters and the changes in wall charge.

Wall voltage transfer curve :

Curve expressed with wall transfer that is caused by any changes in electric charges including wall charges and wall charge pulse related parameters.

White back :

White coating for minimize absorbing valid gloss, located black contrast improvement layer and fluorescent material.

Write electrode :

(Refer to data electrode.)

Write electrode :

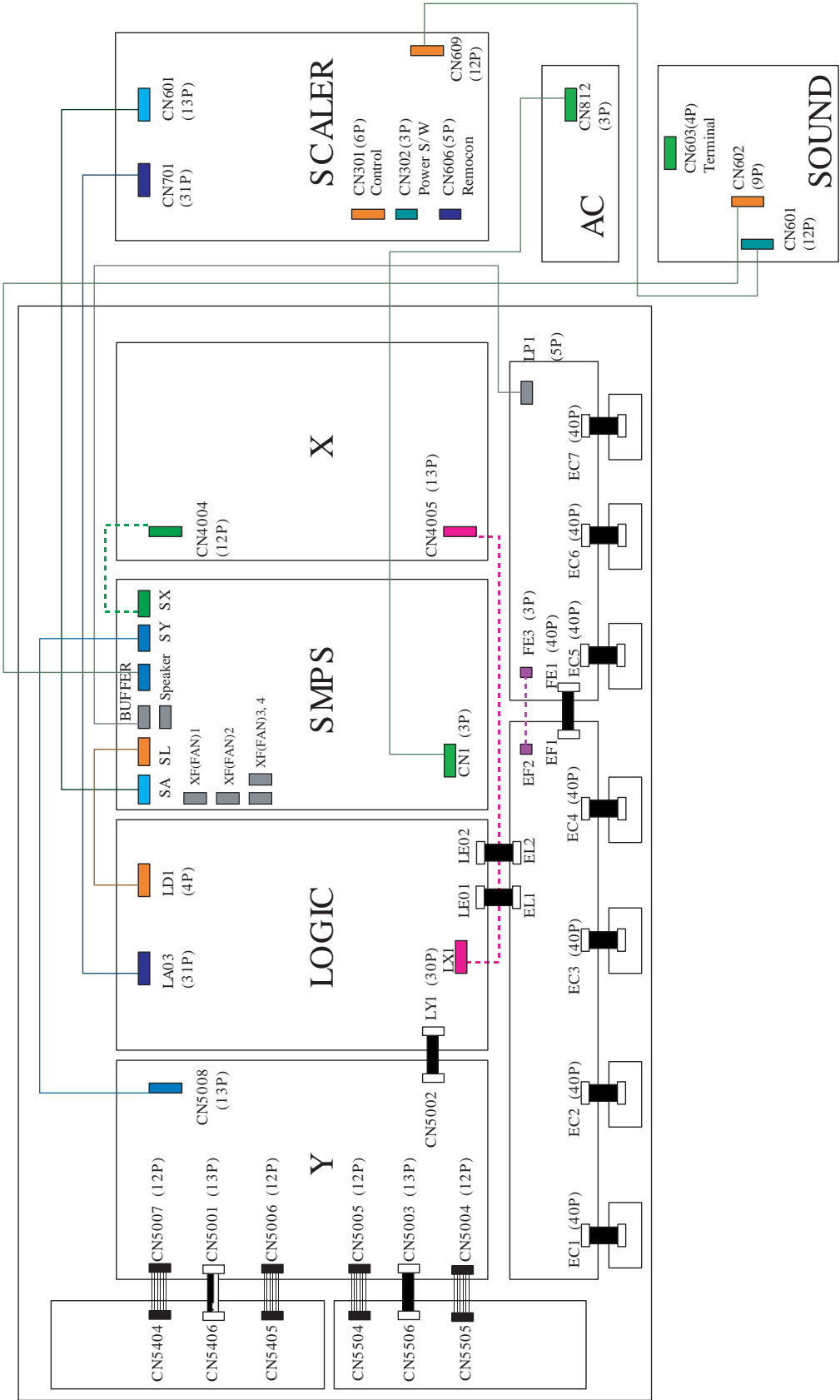
(Refer to data electrode)[symbol : Pw]

Write electrode :

(Refer to data electrode)[symbol : Vw]

MEMO

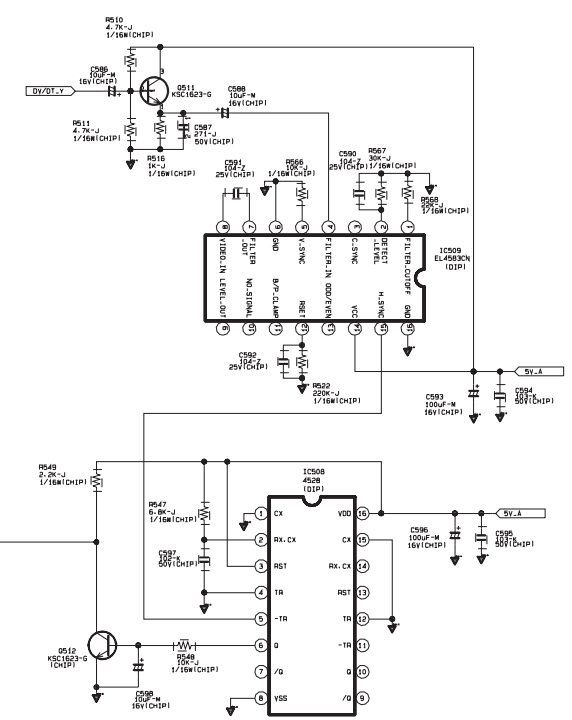
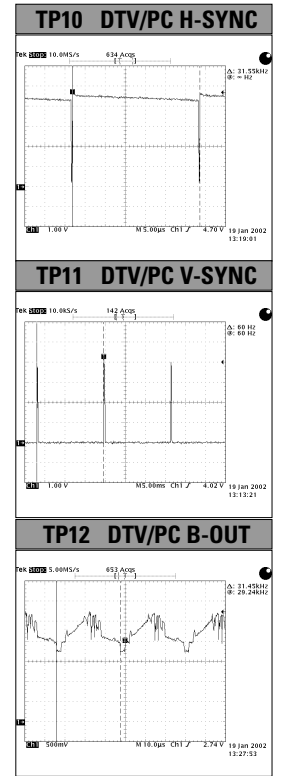
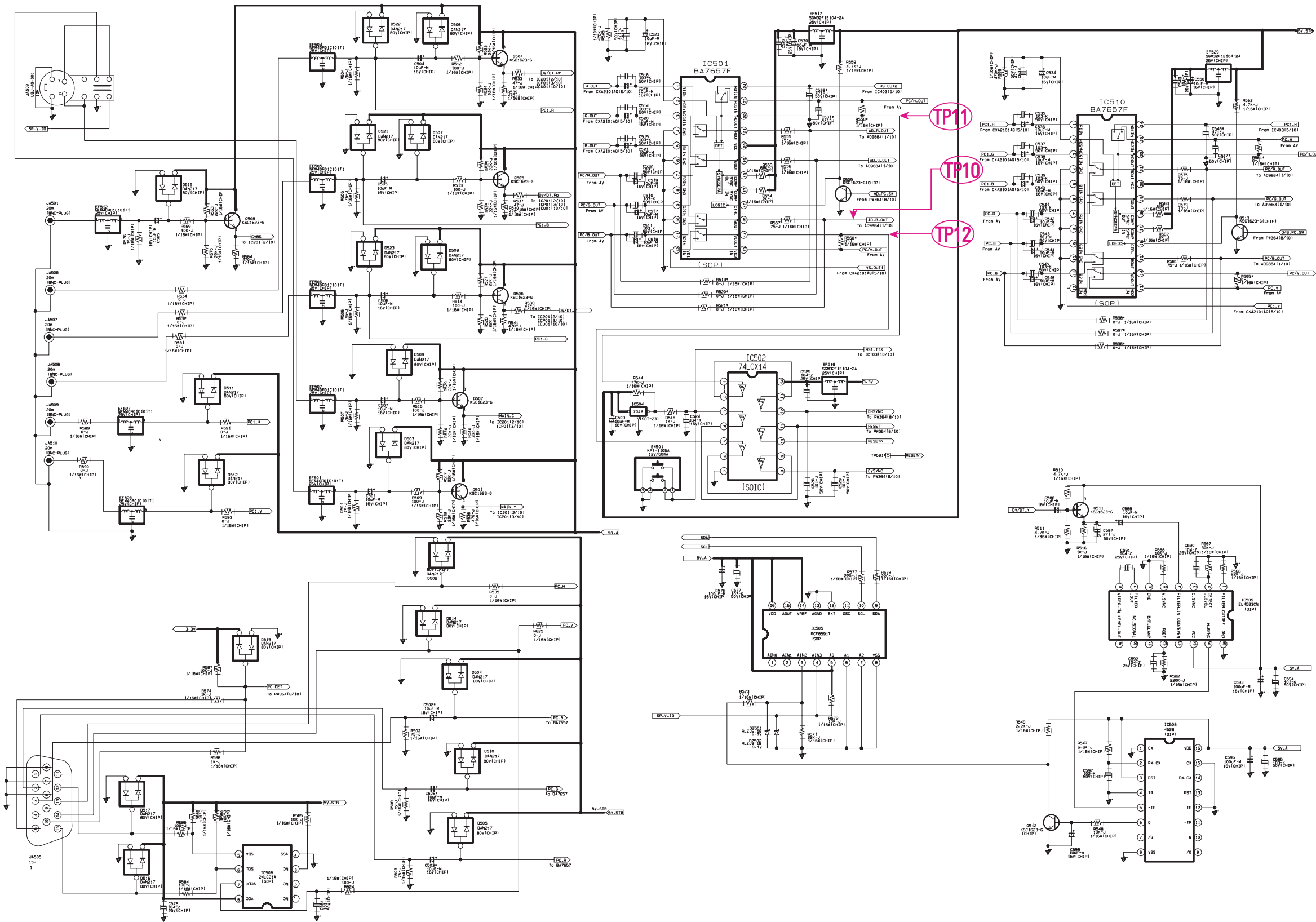
11. Wirng Diagram



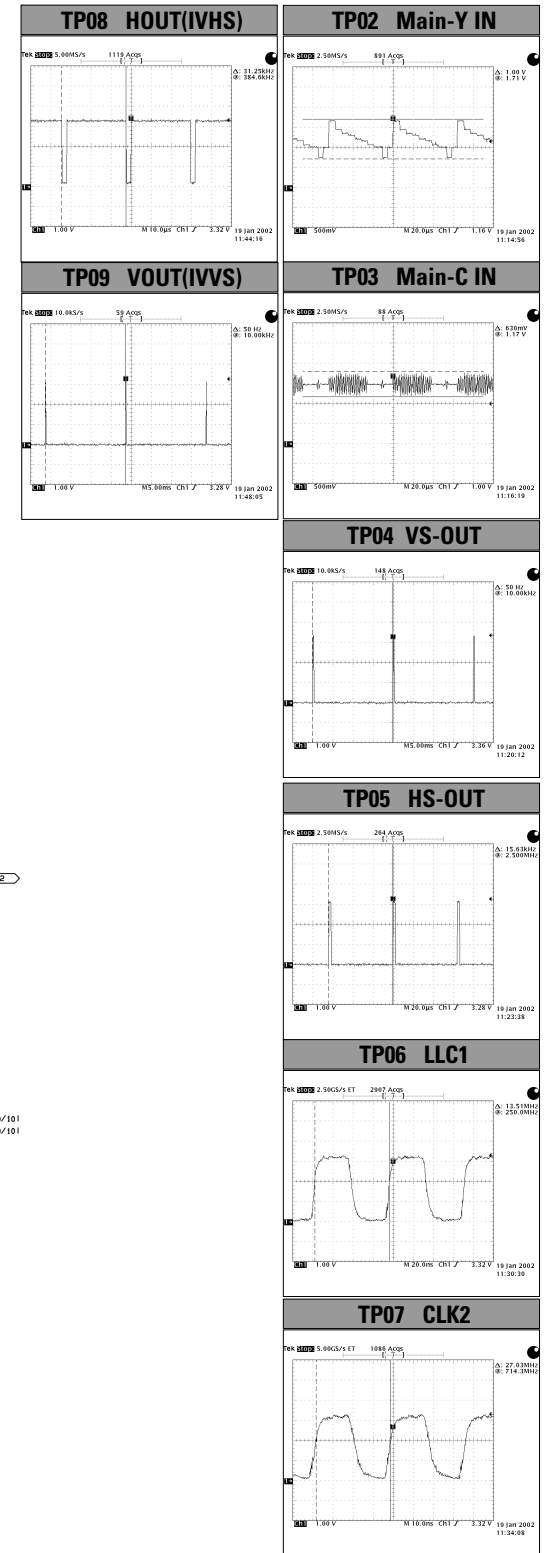
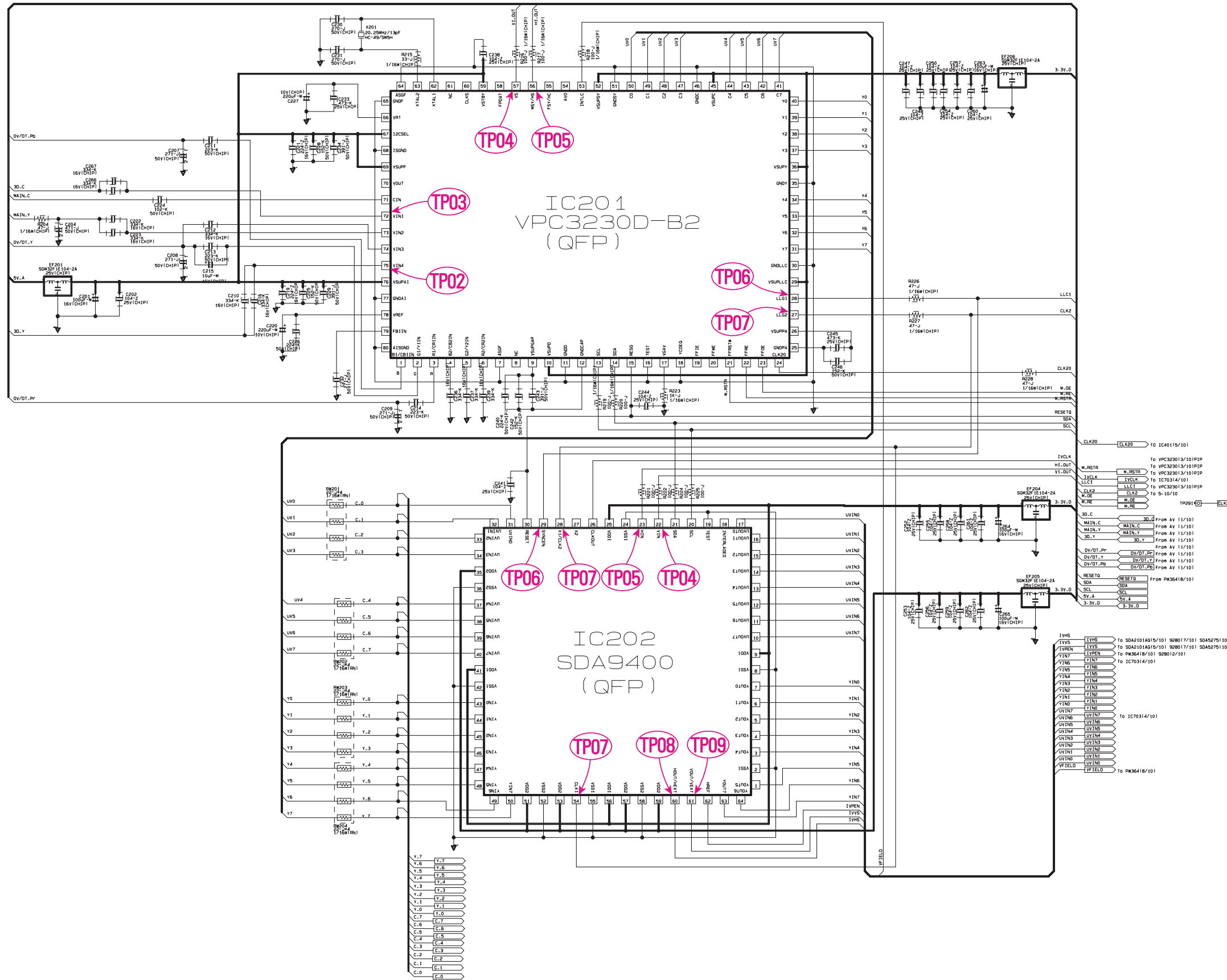
MENO

12. Schematic Diagrams

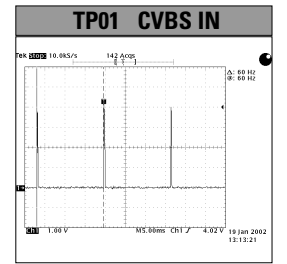
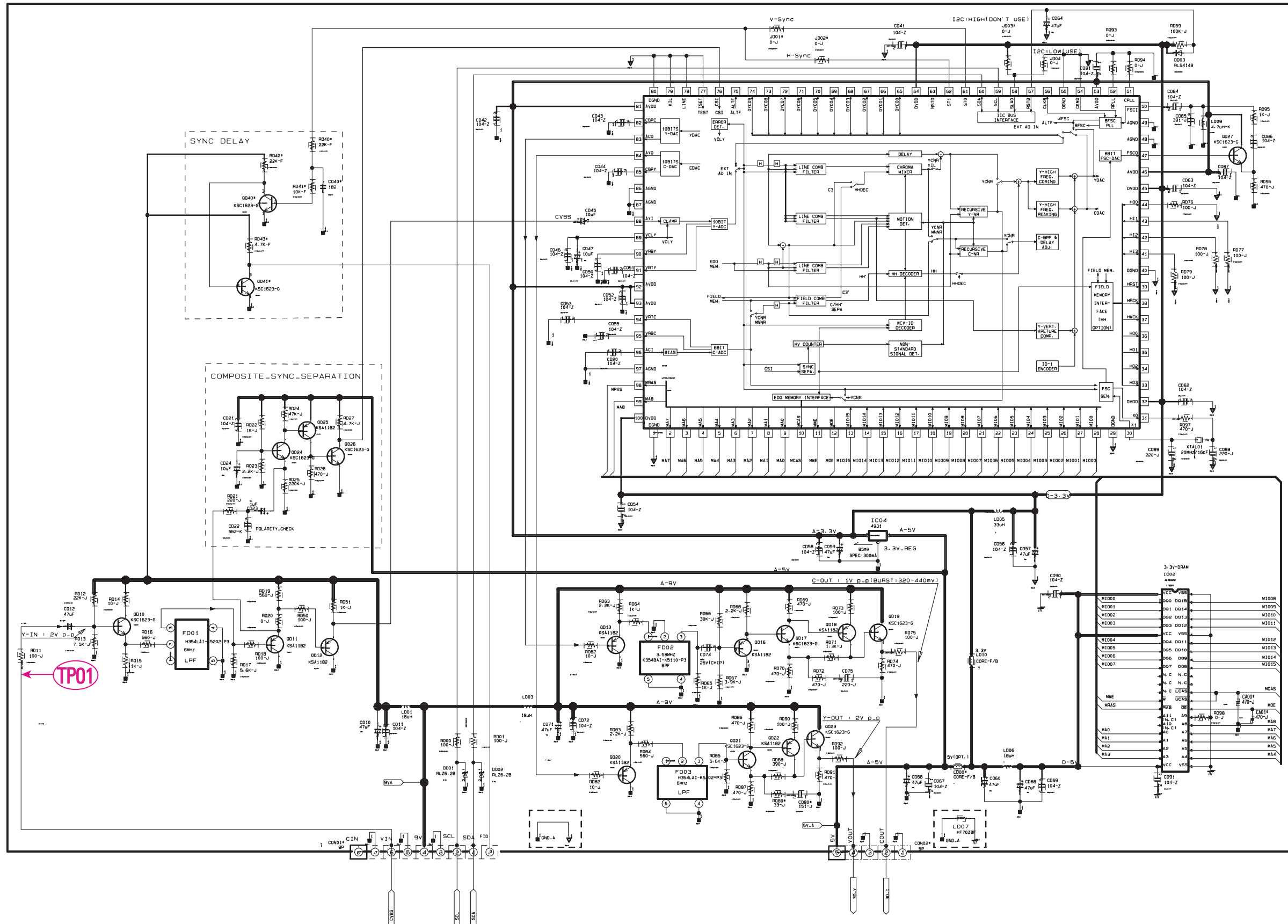
12-1 SCALER1 SIGNAL INPUT, LVDS OUTPUT



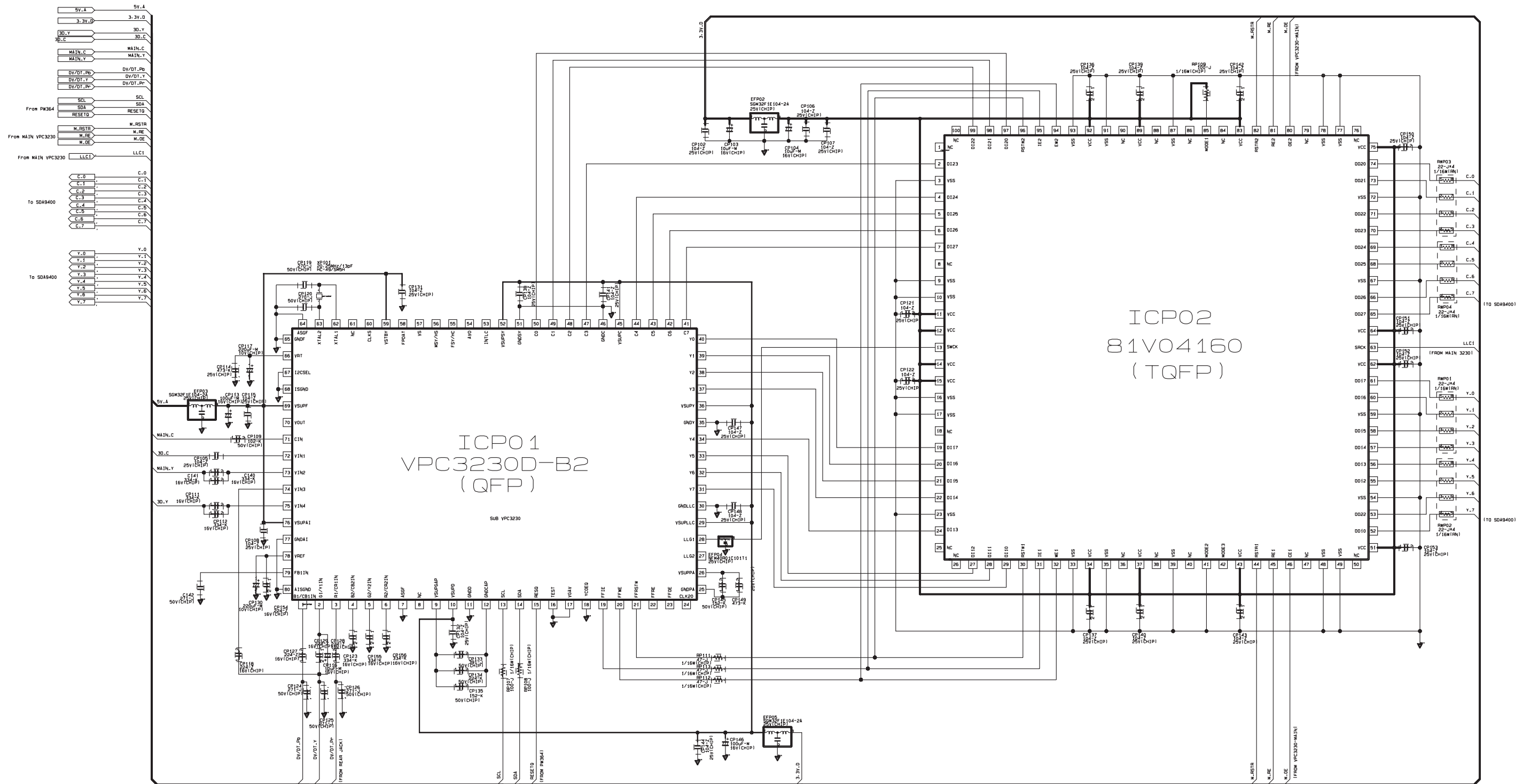
12-2 SCALER2 VIDEO DECODER MAIN, PROGRESSIVE CON.



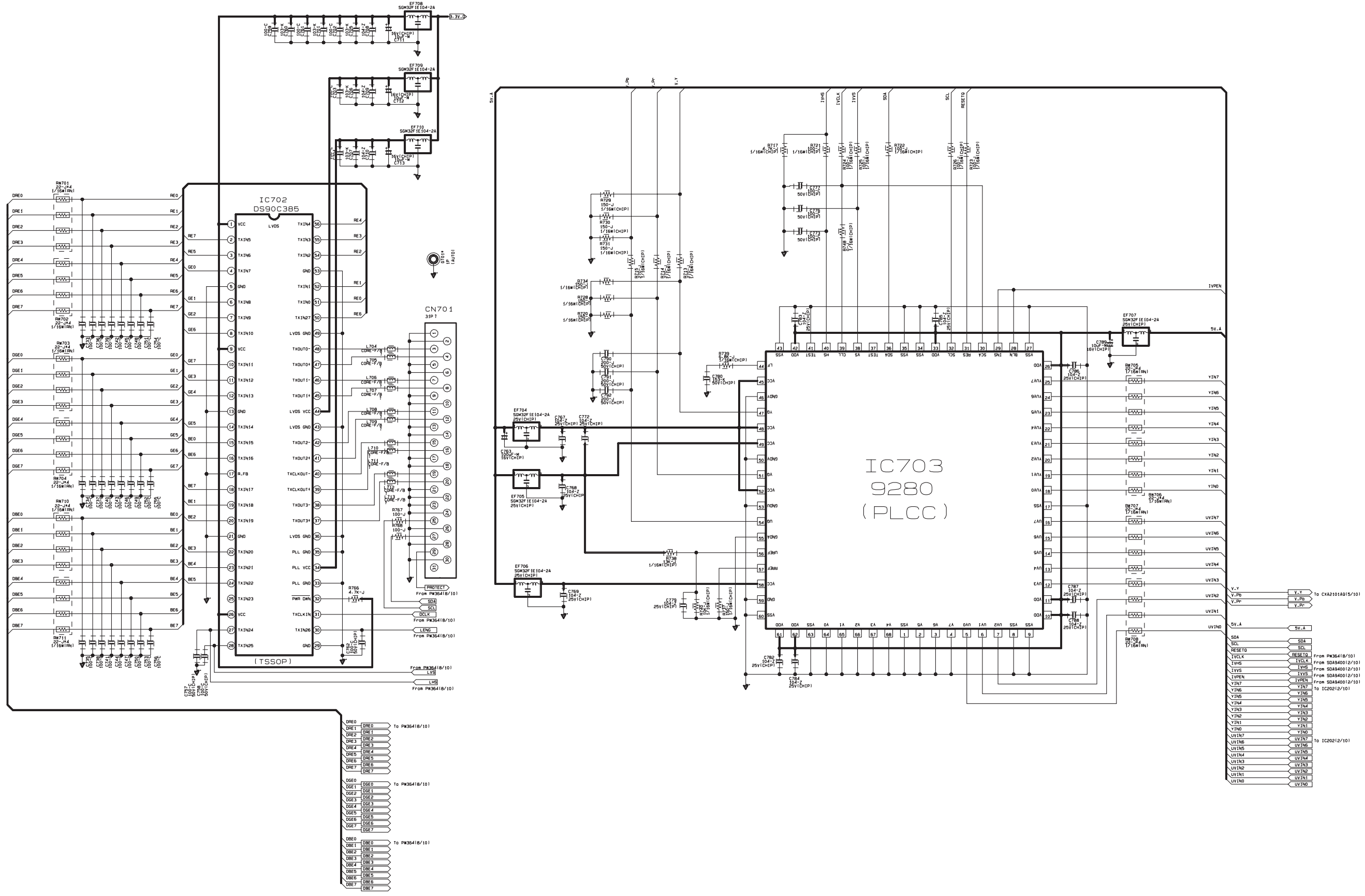
12-3 SCALER3 3D-COMB FILTER



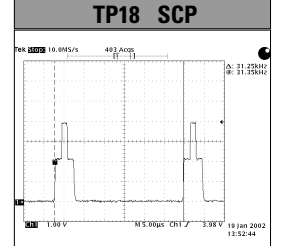
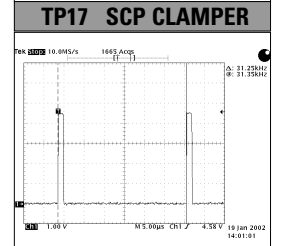
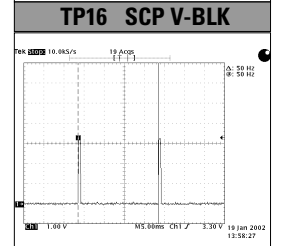
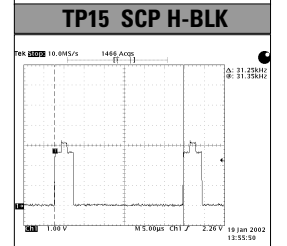
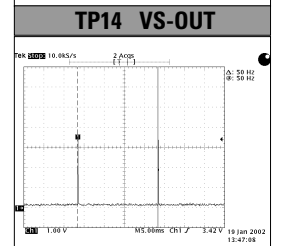
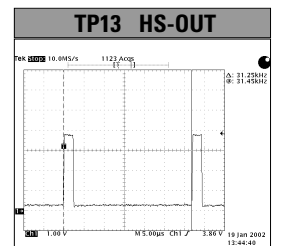
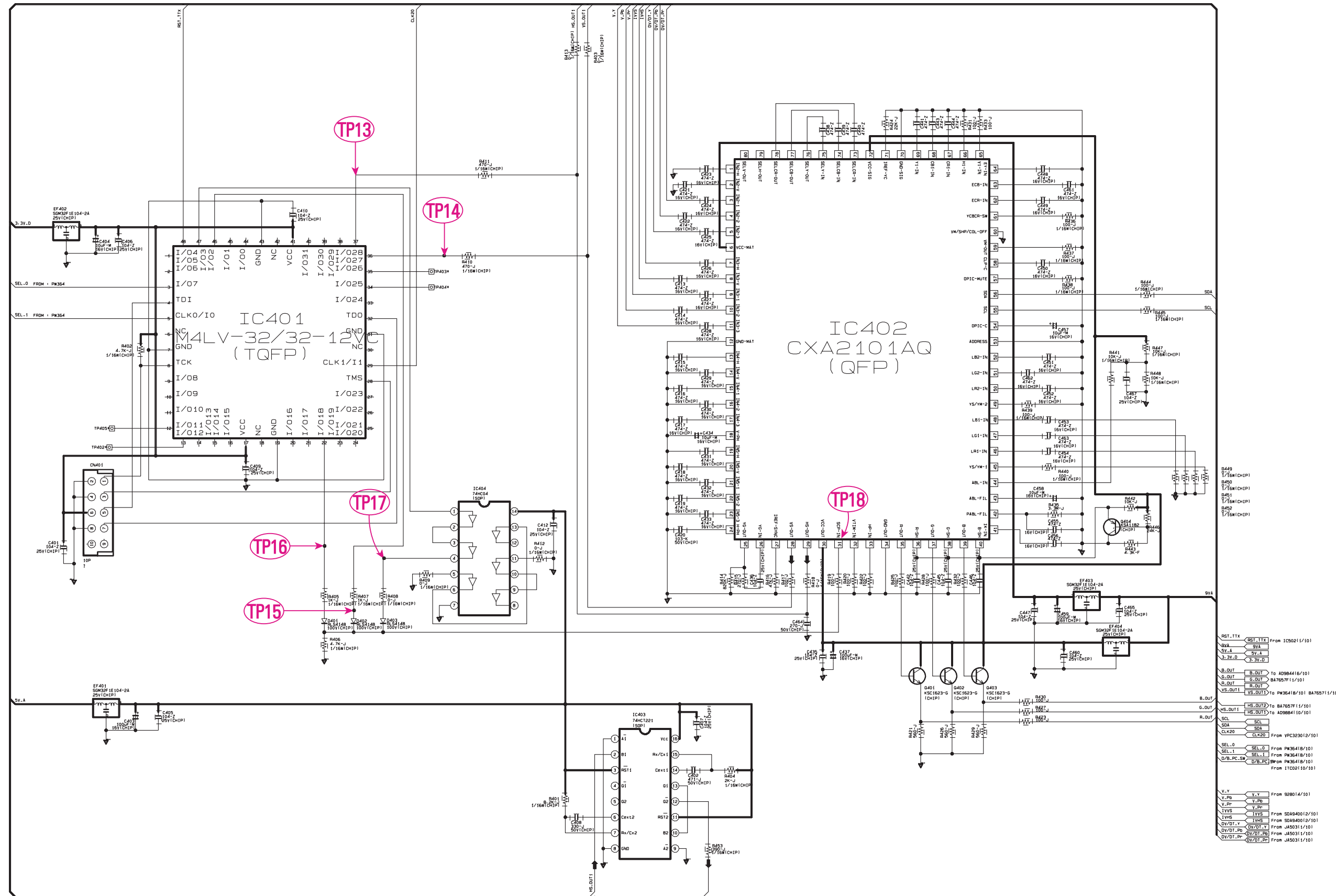
12-4 SCALER4 VIDEO DECODER PIP, FIRST IN/OUTPUT



12-5 SCALERS5 VIDEO DA CON.

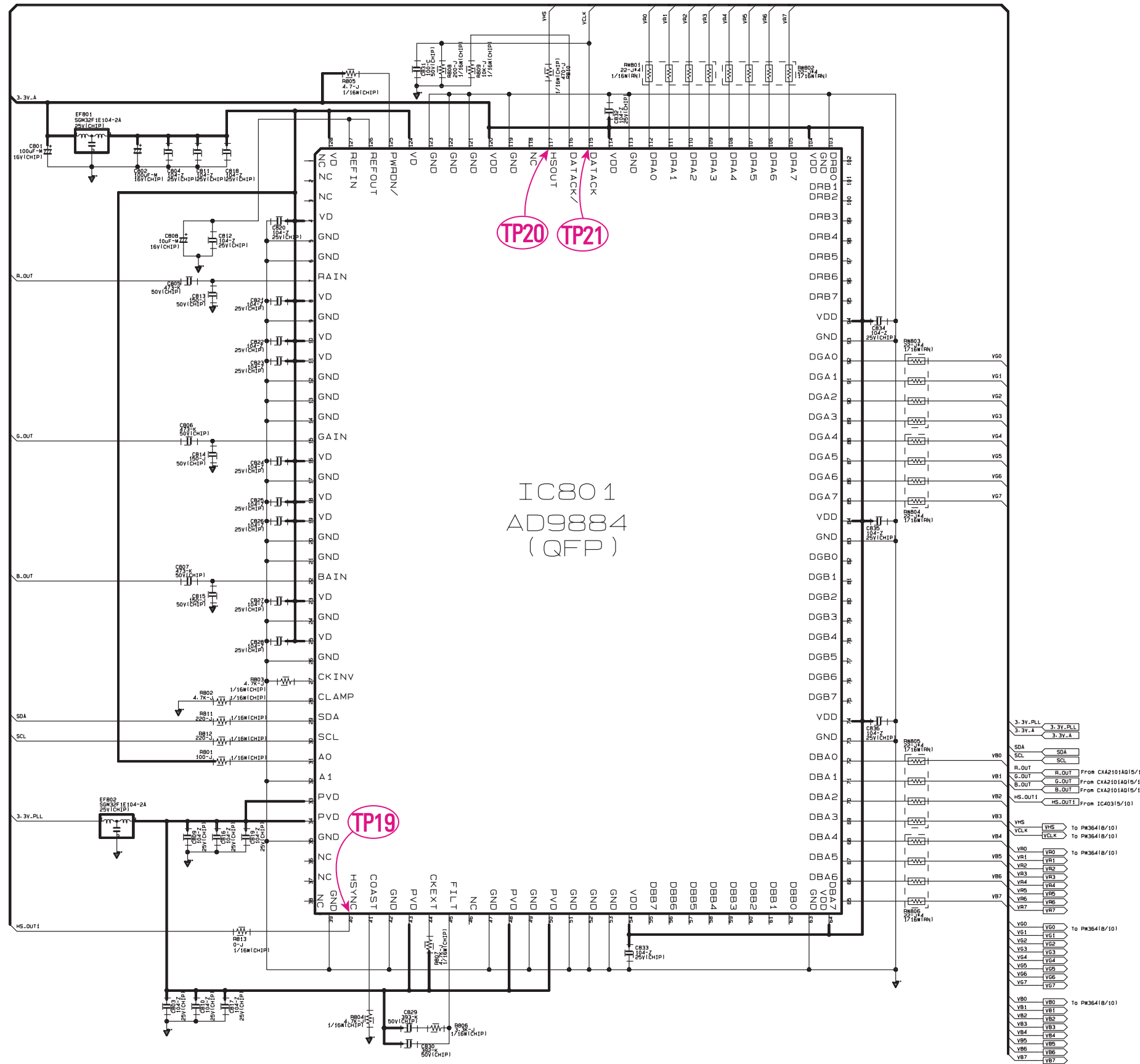


12-6 SCALER6 VIDEO PROCESSOR, SAND CASTLE PULSE GEN.



- RST_1TX From IC50211/101
- 9VA 9VA
- 3.3V_D 3.3V_D
- B_OUT B_OUT To A098416/101
- G_OUT G_OUT BA7657F1/101
- R_OUT R_OUT
- VS_OUT1 VS_OUT1 To PW364(B/10) BA765711/101
- VS_OUT2 VS_OUT2 To BA7657F1/101
- VS_OUT3 VS_OUT3 To A098416/101
- SCL SCL
- SDA SDA
- CLK20 CLK20 From VPC333012/101
- SEL_0 SEL_0 From PW364(B/10)
- SEL_1 SEL_1 From PW364(B/10)
- D/B_PC_3B D/B_PC_3B From PW364(B/10)
- V_V V_V From 928014/101
- V_PG V_PG
- V_PG V_PG
- LVS LVS From S04840012/101
- LVS LVS
- ITVS ITVS From S04840012/101
- ITVS ITVS
- DV/DI_V DV/DI_V From J450311/101
- DV/DI_PD DV/DI_PD From J450311/101
- DV/DI_PC DV/DI_PC From J450311/101

12-7 SCALER7 ADC(VIDEO)

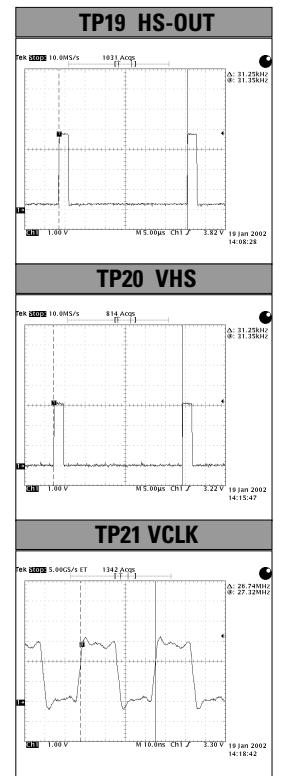


TP20

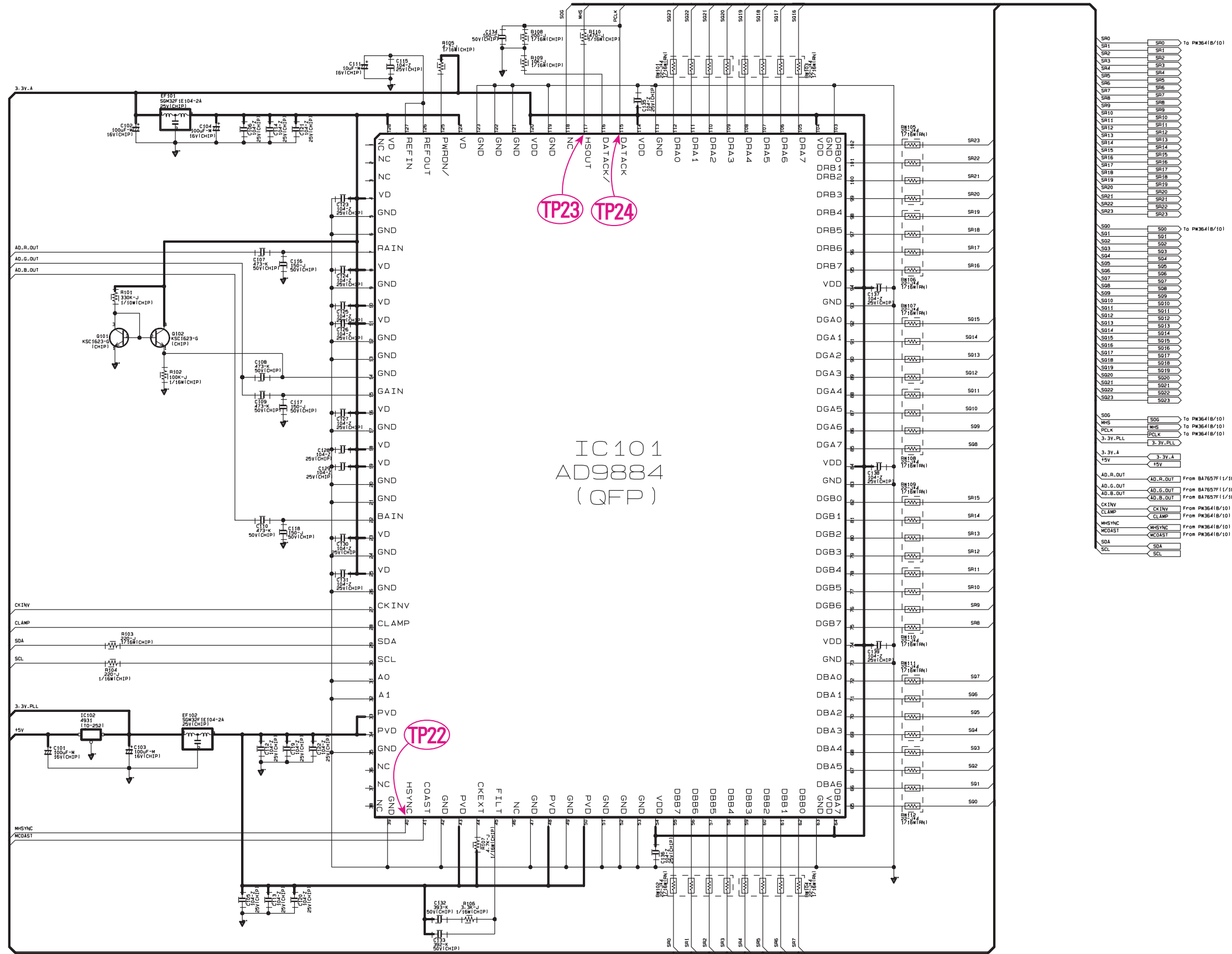
TP21

IC801
AD9884
(QFP)

TP19



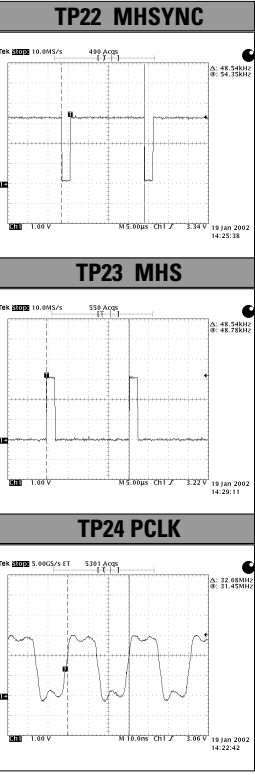
12-8 SCALER8 ADC(PC)



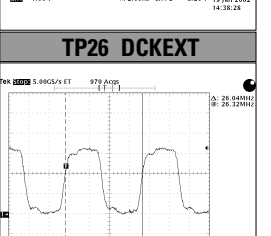
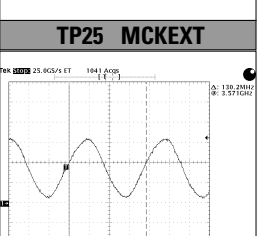
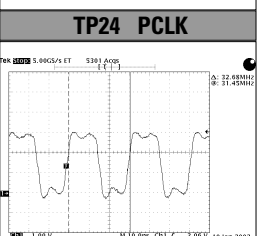
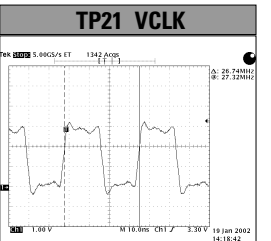
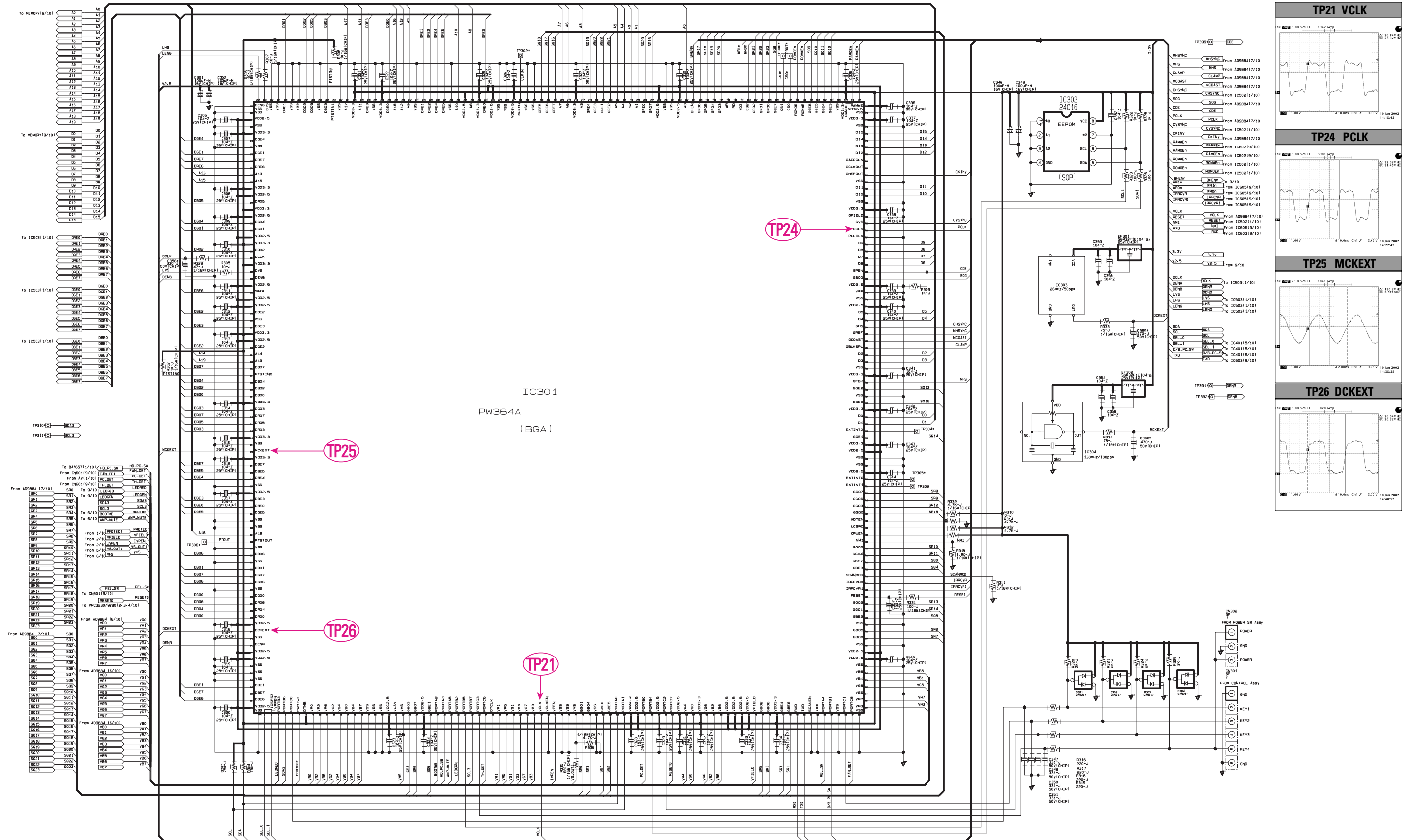
TP23 TP24

IC101
AD9884
(QFP)

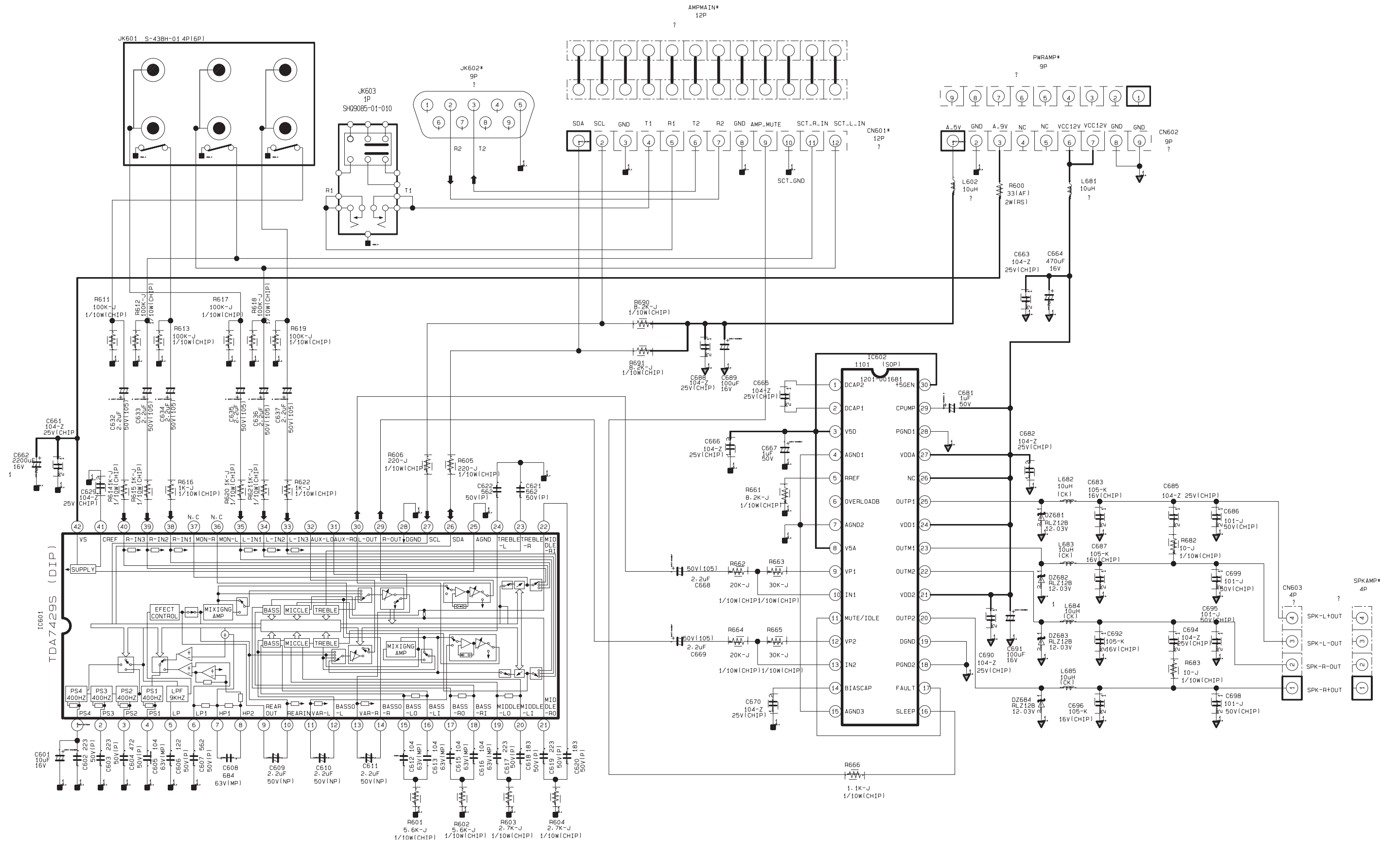
SR0	SR0	To PW3641B/101
SR1	SR1	
SR2	SR2	
SR3	SR3	
SR4	SR4	
SR5	SR5	
SR6	SR6	
SR7	SR7	
SR8	SR8	
SR9	SR9	
SR10	SR10	
SR11	SR11	
SR12	SR12	
SR13	SR13	
SR14	SR14	
SR15	SR15	
SR16	SR16	
SR17	SR17	
SR18	SR18	
SR19	SR19	
SR20	SR20	
SR21	SR21	
SR22	SR22	
SR23	SR23	
S00	S00	To PW3641B/101
S01	S01	
S02	S02	
S03	S03	
S04	S04	
S05	S05	
S06	S06	
S07	S07	
S08	S08	
S09	S09	
S10	S10	
S11	S11	
S12	S12	
S13	S13	
S14	S14	
S15	S15	
S16	S16	
S17	S17	
S18	S18	
S19	S19	
S20	S20	
S21	S21	
S22	S22	
S23	S23	
S00	S00	To PW3641B/101
MHS	MHS	To PW3641B/101
PCLK	PCLK	To PW3641B/101
3.3V_PLL	3.3V_PLL	
1.5V	1.5V	
AD_R_OUT	AD_R_OUT	From BA7657F (1/101)
AD_G_OUT	AD_G_OUT	From BA7657F (1/101)
AD_B_OUT	AD_B_OUT	From BA7657F (1/101)
CK_INV	CK_INV	From PW3641B/101
CLAMP	CLAMP	From PW3641B/101
MHSYNC	MHSYNC	From PW3641B/101
MDCAST	MDCAST	From PW3641B/101
SDA	SDA	
SCL	SCL	



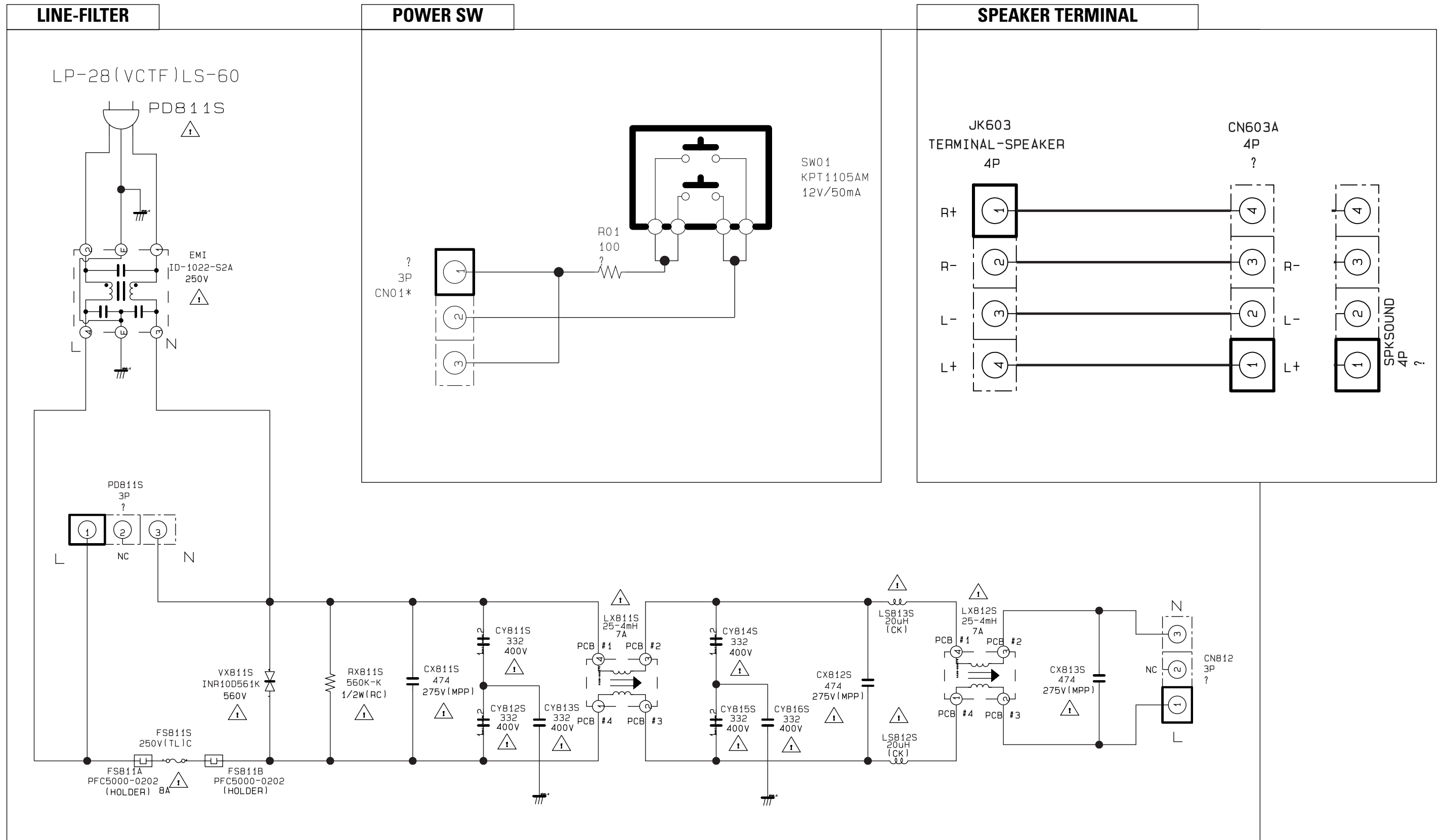
12-9 SCALER9 PW364



12-11 SOUND



12-12 LINE-FILTER, POWER SW, SPEAKER TERMINAL



12-13 CONTROL, REMOCON

